2. Sep. 1981

2816
16K (2K x 8) ELECTRICALLY ERASABLE PROM

- **HMOS*-E FLOTOX Cell Design**
- **Reliable Floating Gate Technology**
- **Very Fast Access Time:**
  —2816, 250 ns Max.
  —2816-3, 350 ns Max.
  —2816-4, 450 ns Max.
- **Single Byte Erase/Write Capability**
- **10 ms Byte Erase/Write Time**
- **Chip Erase Time of 10 ms**
- **Conforms to JEDEC Byte-Wide Family Standard**
- **Microprocessor Compatible Architecture**
- **Low Power Dissipation:**
  —Active Current, 110 mA Max.
  —Standby Current, 50 mA Max.
- **Erase/Write Specifications Guaranteed 0-70°C**

The Intel® 2816 is a 16,384 bit electrically erasable programmable read-only memory (E^2PROM). The 2816 can be easily erased and reprogrammed on a byte basis. A chip erase function is also provided. The device operates from a 5-volt power supply in the read mode; writing and erasing are accomplished by providing a single 21-volt pulse.

The 2816, with its very fast read access speed, is compatible with high performance microprocessors such as the 8086-2. Using the fast access speed allows zero wait operation in large system configurations.

The electrical erase/write capability of the 2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write. Never before has in-system alterability been possible with this combination of density, performance and flexibility. Any byte can be erased or written in 10 ms without affecting the data in any other byte. Alternatively, the entire memory can be erased in 10 ms allowing the total time to rewrite all 2K bytes to be cut by 50%. The 2816 provides a significant increase in flexibility allowing new applications (dynamic reconfiguration, continuous calibration) never before possible.

The 2816 E^2PROM possesses Intel's 2-line control architecture to eliminate bus contention in a system environment. A power down mode is also featured; in the standby mode power consumption is reduced by over 55% without increasing access time. The standby mode is achieved by applying a TTL-high signal to the CE input.

Byte erase and write are controlled entirely by TTL signal levels, yet require no control signals beyond $\overline{CE}$ and $\overline{OE}$. For byte write a selected chip ($\overline{CE}$ = TTL low) senses the 21V V_{PP} pulse and automatically goes into write mode. Byte erase mode is identical to byte write except that data-in must be all logic ones (TTL-high). Never before has an in-system alteration of non-volatile information been implemented with such simple control.

*HMOS-E is a patented process of Intel Corporation.

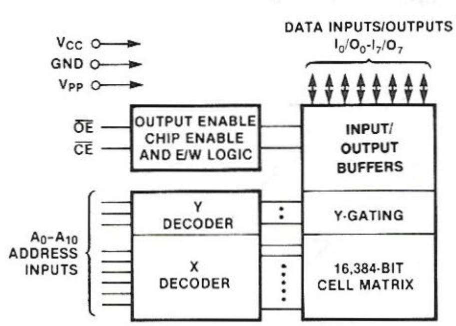
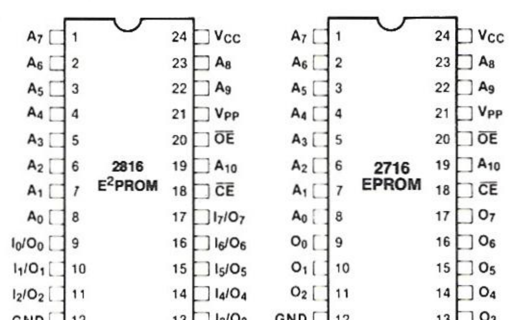


Figure 1. 2816 Functional Block Diagram



PIN NAMES	
A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	DATA OUTPUTS
I_0-I_7	DATA INPUTS
V_{PP}	PROGRAM VOLTAGE

Figure 2. Pin Configuration

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DEVICE OPERATION

The 2816 has six modes of operation, listed in Table 1. All operational modes are designed to provide maximum microprocessor compatibility and system consistency. The device pinout is a part of Intel's JEDEC approved byte wide Non-Volatile Memory family, allowing appropriate and cost-effective density and functionality upgrades.

All control inputs are TTL compatible with the exception of chip erase. The V_{PP} voltage must be pulsed to 21 volts during write and erase, and held to 4 to 6 volts during the other two modes.

Table 1. Mode Selection $V_{CC}=+5V$

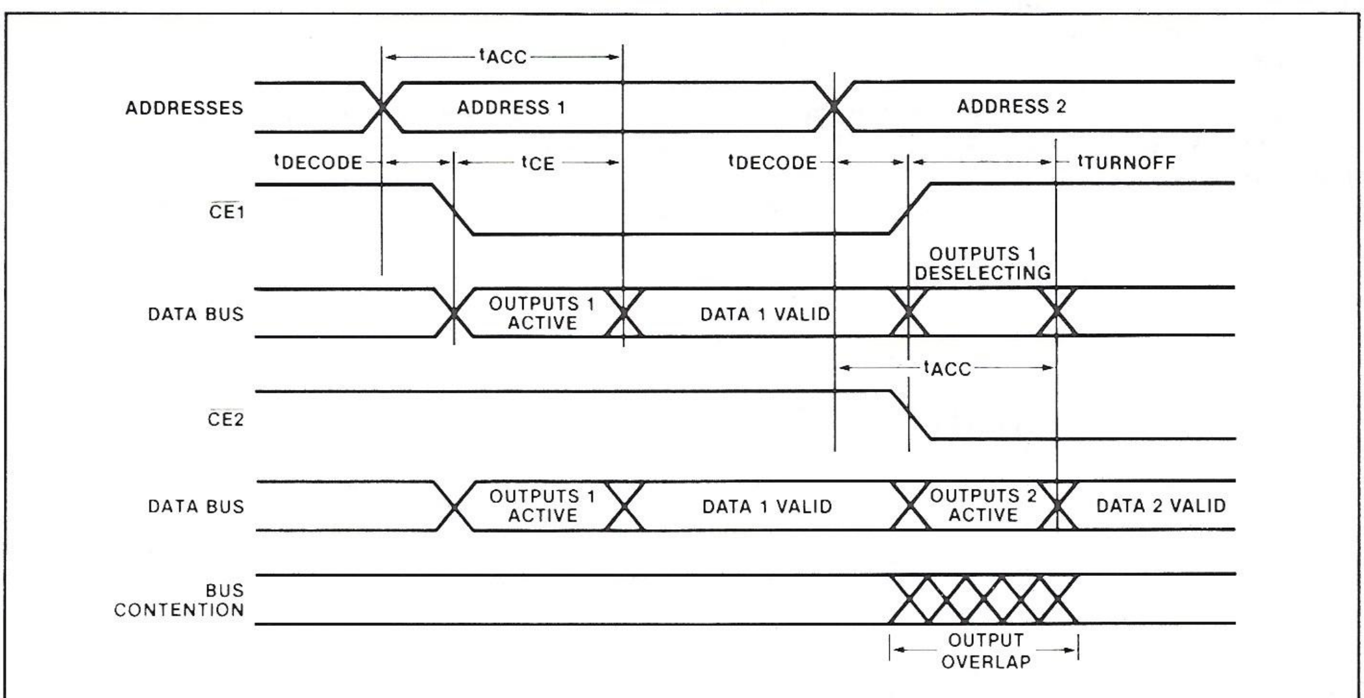
MODE \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	V_{PP} (21)	INPUTS/ OUTPUTS
READ	V_{IL}	V_{IL}	+4 to +6	D_{OUT}
STANDBY	V_{IH}	DON'T CARE	+4 to +6	HIGH Z
BYTE ERASE	V_{IL}	V_{IH}	+21	$D_{IN}=V_{IH}$
BYTE WRITE	V_{IL}	V_{IH}	+21	D_{IN}
CHIP ERASE	V_{IL}	+9 to +15V	+21	[10] $D_{IN}=V_{IH}$
E/W INHIBIT	V_{IH}	DON'T CARE	+4 to +22V	HIGH Z

Read Mode

Optimal system efficiency depends to a great extent on a tightly coupled microprocessor/memory interface. The E^2PROM device should respond rapidly with data to allow the highest possible CPU performance. The 2816 satisfies this high performance requirement because of access times typically less than 250 ns. Program execution directly out of electrically erasable memory has never before been possible; the 2816 opens this new, powerful applications segment.

The 2816 uses Intel's proven 2-line control architecture for read operation. Figure 3 shows the timing disadvantages of a single-line control architecture. 2-line control, shown in Figure 4, has been developed by Intel to solve this bus contention and the associated system reliability problems. Both $\overline{CE}$ and $\overline{OE}$ must be at logic low levels to obtain information from the device. Chip enable ($\overline{CE}$) is the power control pin and should be used for device selection. The output enable ($\overline{OE}$) pin serves to gate internal data to the output pins. Assuming that the address inputs are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a time delay of t_{OE}, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Figure 5 shows a typical system interconnection. Here the 2816 contains program information that the 8086 requires for system function.



For footnotes see page 13.

Figure 3. Single-Line Control and Bus Contention

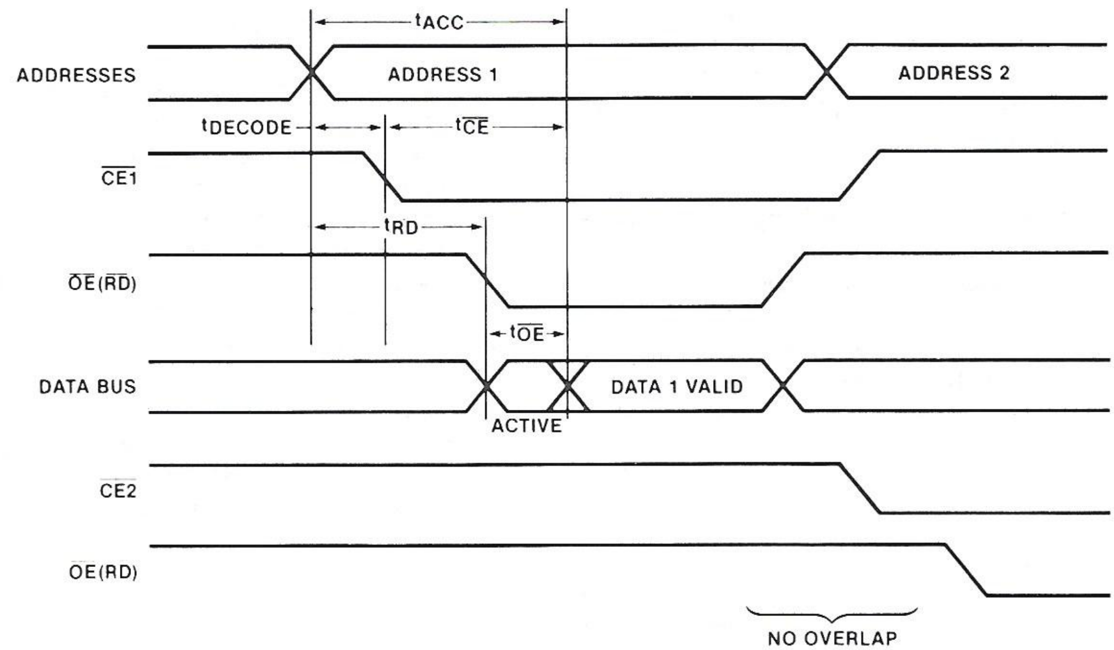


Figure 4. Two-Line Control Architecture

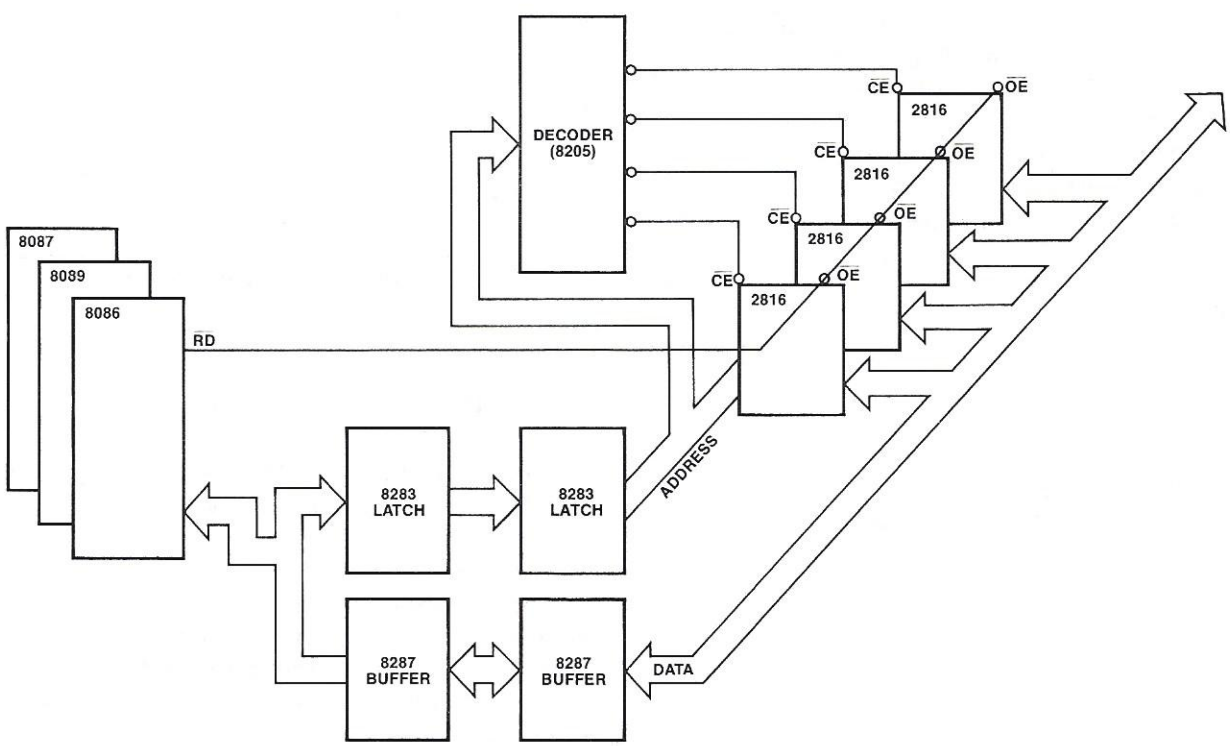


Figure 5. iAPX 86/2816 Read Architecture

For footnotes see page 13.

Write Mode

The 2816 is erased and reprogrammed electrically rather than optically, as opposed to EPROMs which require UV light. The device offers dramatic flexibility because both byte (single location) and chip erase are possible.

A close examination of the broad application spectrum for the E^2 device reveals an inherent need for single location erase capability. Program store applications can be classified in several ways. Figure 6 lists various storage modes and the required erase function. In greater than 80% of all cases, a byte erase feature is necessary. See AP-106 for details.

APPLICATION TYPE	IDEAL ERASE MODE
• Strict Program Store	CHIP
• Relocatable Program Structures	BYTE
• Program Store Extension	BYTE
• Program Execution Constants	BYTE
• Program Dependent Data Store	BYTE
• Data Store Applications	BYTE

Figure 6. Microprocessor Storage Types

To write a particular location, that byte must be erased prior to a data write. Erasing is accomplished by applying logic 1 (TTL-high) inputs to the data input pins, lowering $\overline{CE}$, and applying a 21-volt programming signal to V_{PP}. The $\overline{OE}$ pin must be held at V_{IH} during byte erase and write operations. The programming pulse width must be a minimum of 9 ms, and a maximum of 15. The rising edge of V_{PP} must conform to the RC time constant specified above. Once the location has been erased, the same operation is repeated for a data write. The input pins in this case reflect the byte that is to be stored.

A characteristic of all E^2PROMs is that the total number of erase/write cycles is not unlimited. The 2816 has been designed and manufactured to meet applications requiring up to 1×10^4 erase/write cycles per byte. The erase/write cycling characteristic is completely byte independent. Adjacent bytes are not affected during erase/write cycling.

Because the device is designed to be written in system, all data sheet specifications (including write and erase operations) hold over the full operating temperature range (0-70°C).

For footnotes see page 13.

CONTROLLERS

Controller I Description

The Controller I interface provides the lowest cost, smallest P.C. board space implementation, though it is unable to offer the maximum CPU throughput capability since wait states are inserted into the memory cycle during the 10 ms write time. Figure 7 shows the block diagram for this implementation. A timer device is provided to time 10 ms, which connects directly to the CPU READY line. When activated, the timer engages the V_{PP} switch, locks the CPU address, data, and control bus, and writes the 2816. After completion of the write cycle, the CPU is relinquished to do other tasks. Such a control application is appropriate when the processor can be dedicated to the write, such as in program store.

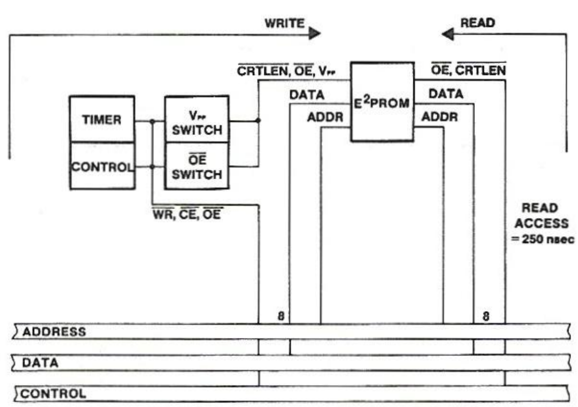


Figure 7. Controller I

Controller II Description

To provide a higher CPU throughput capability, the interface shown in Figure 8 was designed. In this case, all latching and timing signals are generated by discrete devices. The CPU simply sends a write operation to the interface as it would to a RAM device. After the CPU has engaged the write sequence, it is free to perform other tasks not related to 2816 control. At the completion of the write cycle, the interface interrupts the CPU which then vectors to an interrupt service routine. Controller II offers real-time CPU performance with a high degree of hardware overhead.

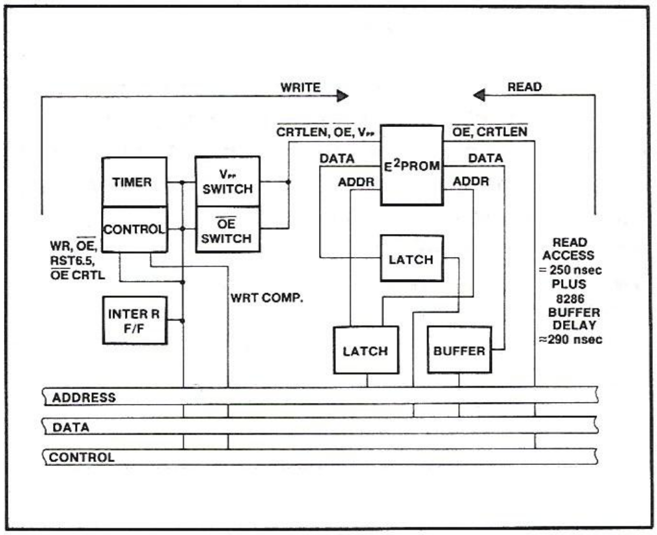


Figure 8. Controller II

Controller III Description

The Controller III implementation was designed to provide the real-time processing capability of Controller II, without the large hardware overhead. See Figure 9. In this design an Intel 8155 I/O port timer device is used to advantage. The ports provide the latching of data and address during the write cycle, while the timer performs accurate pulsing of the V_{PP} for the required duration. Much of the hardware has been reduced through the 8155. The interrupt structure of Controller II is used as well. Read access is very fast despite a multiplexer and a buffer delay.

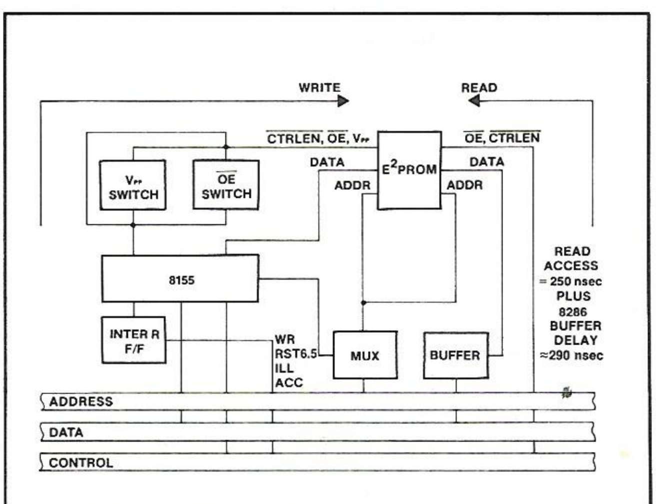


Figure 9. Controller III

Controller IV Description

Data store applications were in mind for the Controller IV design shown in Figure 10. In this case, read access was not a concern, though write erase access and hardware overhead were exceptionally important. This controller takes the 2816 completely off-line for both read and write operations. The write cycle is accomplished in the same way as in Controller III. Reading, however, is accomplished through several I/O operations.

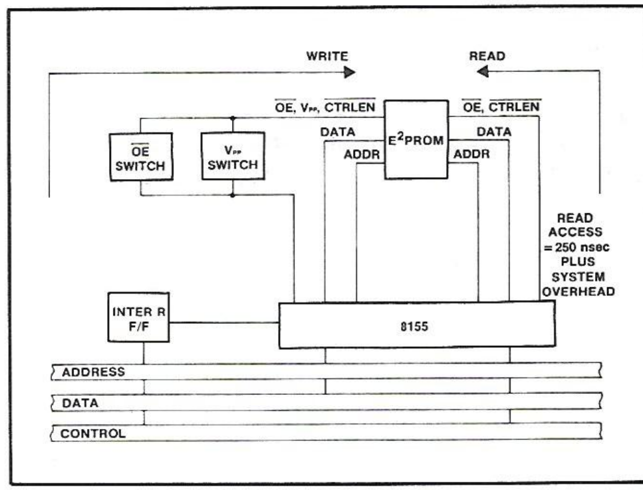


Figure 10. Controller IV

Chip Erase Mode

Should one wish to erase the entire 2816 array at once, the device offers a chip erase function. When the chip erase function is performed all 2K bytes are returned to a logic 1 (FF) state.

The 2816's chip erase function is engaged when the output enable ($\overline{OE}$) pin is raised above 9 volts. When $\overline{OE}$ is greater than 9 volts and $\overline{CE}$ and V_{PP} are in the normal write mode, the entire array is erased. This chip erase function takes approximately 10 ms. The data input pins must be held to a TTL high level during this time. Figure 11 is a recommended $\overline{OE}$ control switch.

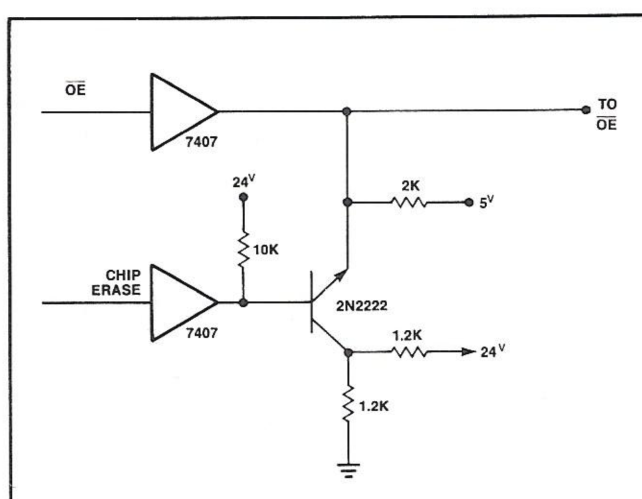


Figure 11. $\overline{OE}$ Chip Erase Control

For footnotes see page 13.

V_{PP} Pulse

The shape of the V_{PP} pulse is important in ensuring long term reliability and operating characteristics. V_{PP} must rise to 21V through an RC waveform (exponential). The T_{PRC} specification has been designed to accommodate changes of RC due to temperature variations.

Figure 12a shows a recommended V_{PP} switch design, useful where programming will occur over the specified temperature and operating voltage conditions.

Voltage Generation

The Intel 2816 is a new generation of non-volatile memory in which writing and erasing can be accomplished on board by providing a 21 volt pulse. In order to generate the V_{PP} pulse, a power supply with output voltage of +24V is needed. In a system environment where this voltage is not available, a switching regulator can be used to convert +5V to +24V. Figure 12b shows the circuit diagram for such a voltage converter. In systems where 24 volts is not available, this circuit proves to be a cost effective alternative.

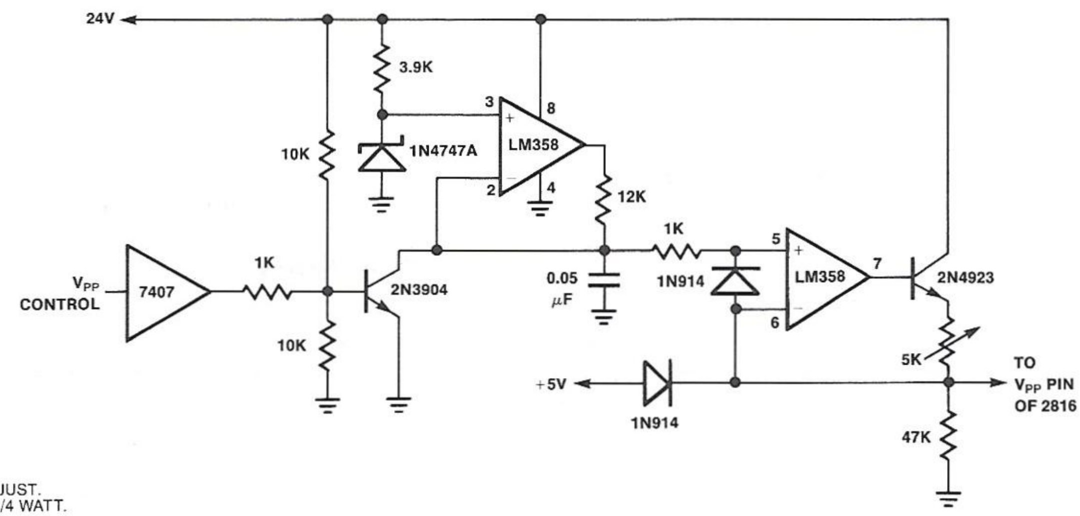


Figure 12a. Operational Amplifier V_{PP} Switch Design[12]

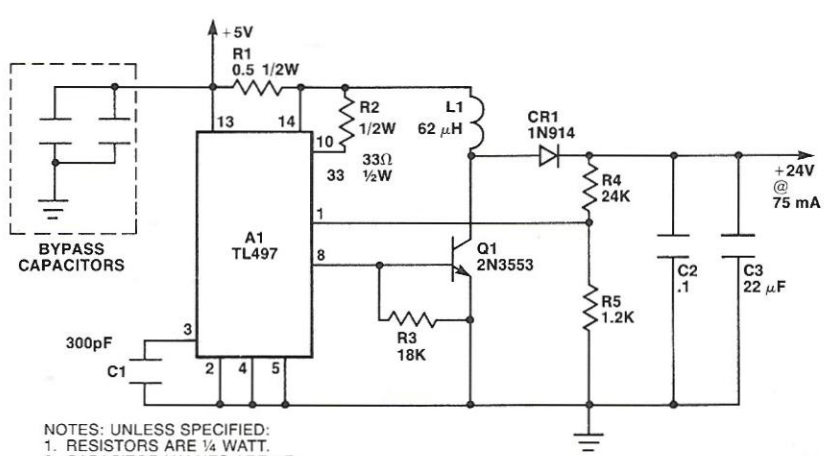


Figure 12b. Step-up Regulator Converts +5V Into +24V

For footnotes see page 13.

Applications

The 2816 E^2PROM is a new and powerful addition to the non-volatile family. It offers a high degree of RAM-like flexibility while retaining the non-volatile characteristics of ROM.

Because of these device parameters, the device is ideal for new and future designs as well as a replacement for existing ROM devices. Some of these potential uses are listed below:

1. Calibration constants storage (continuous calibration).
2. Software alterable control stores (dynamic reconfiguration).
3. Remote communications programming.
4. PC and NC Industrial Applications.
5. CRT terminal configuration and custom graphic and font sets.
6. Military replacements for core memory and fuse-link PROMs.
7. Point of sale terminals.
8. Remote alterable look-up tables.
9. Printer and communications controllers.
10. Remote data gathering.

Because of these device attributes, applications never before possible can now be realized in high performance, consistent microprocessing systems.

Figures 13, 14, 15, and 16 are block diagrams of some typical applications. These applications are explained as follows:

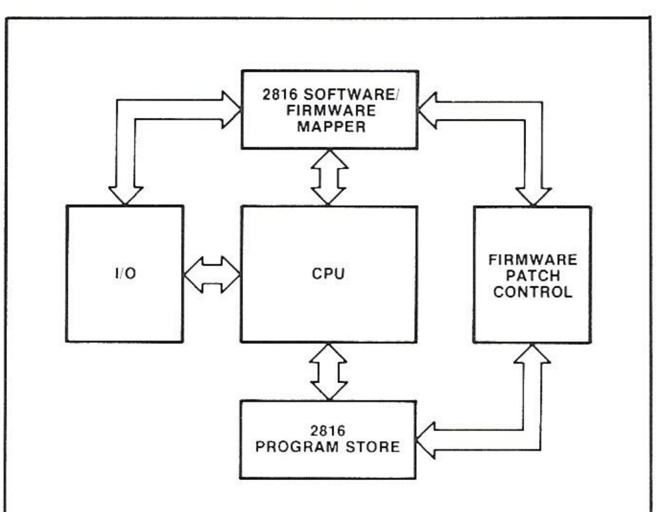


Figure 13. Dynamic Reconfiguration

For footnotes see page 13.

DYNAMIC RECONFIGURATION

The ability of a computer system to alter its operating software while running is now possible with the 2816. The system can monitor external factors, as well as change loop constants, subroutines and other software features in real-time. Figure 13 illustrates this optimal performance. In memory systems, the 2816 can be used to map around hard memory failures in real-time, allowing self-healing memory systems. Such a self-correcting mechanism extends the operating time and reduces service costs to the end user.

CONTINUOUS SELF-CALIBRATION

A high cost of machine service and downtime is due to instrument calibration and readjustments. Use of the 2816 and microprocessor based instruments to contain calibration constants allows features never before possible. See Figure 14. The instrument can now continuously calibrate itself, without expensive downtime in service interaction. The 2816 allows this flexibility and reduction of service costs.

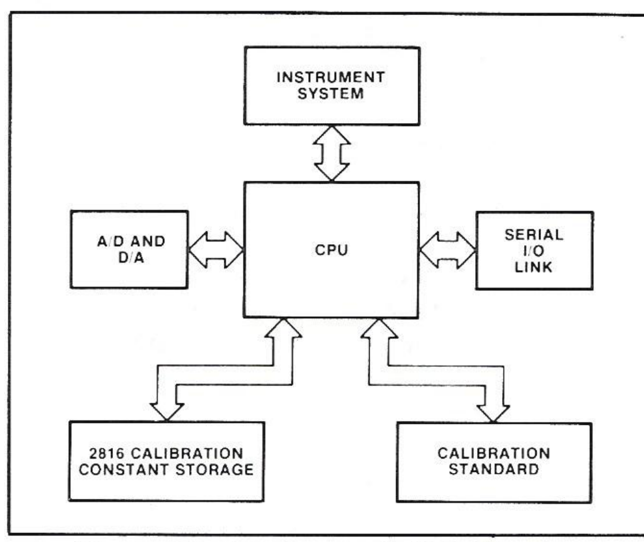


Figure 14. Continuous Self-Calibration

CRT TERMINAL

Custom fonts, graphics characters, and individual configurations can all benefit from the features of the 2816. A CRT terminal, shown in Figure 15, can now be enhanced by using the E^2 as a replacement for jumpers and dip switches. It can also be used as a programmable character generator, and in graphics configuration.

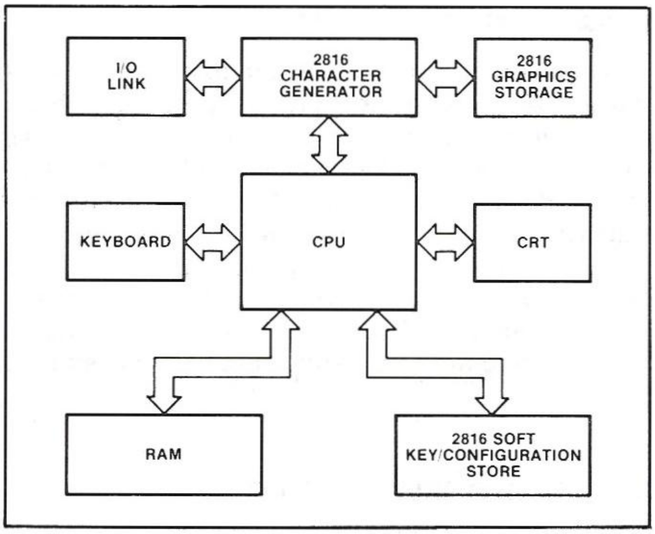


Figure 15. CRT Terminal

POINT OF SALE TERMINAL

Using the 2816 to contain non-volatile price and product descriptions, as shown in Figure 16, is an ideal application in point of sale terminals. With the ability of the 2816 to be altered in-system comes the capability to remotely (over telephone lines) configure the look up table from a central data base computer. The non-volatility of the 2816 is used to advantage as the data store remains intact after power is removed from the system.

Pin Compatibility

The 2816 pinout has been designed for compatibility with present and future memory products. The E^2PROM is a member of Intel's JEDEC standard Byte-Wide memory family which allows density upgrades, functional interchange, and extended product life. Figure 17 shows this JEDEC 28 pin site pinout approach.

Available Literature

To give the system designer an opportunity to more thoroughly understand the device attributes and uses, a library of E^2 information is available. The following list is a brief synopsis:

AP-101—The 2816 Electrical Description

AP-102—2816 Microprocessor Interface Considerations

AP-103—Programming E^2PROM with a Single 5-Volt Power Supply

AP-104—Extending E^2 Endurance—Software Techniques

For footnotes see page 13.

AP-105—Microprocessor Interface—Competitive System Comparisons

AP-106—2816 Byte Erase—Architecture Implications

AP-107—Hardware and Software Download Techniques with 2816

E^2PROM Applications Handbook

To obtain this literature contact your local Field Sales office. In addition, your Field Applications Engineer can discuss with you the controller interfaces for different MPU system configurations.

All of the above literature will be available at the end of Q2 1981. The E^2PROM Applications Handbook is available now.

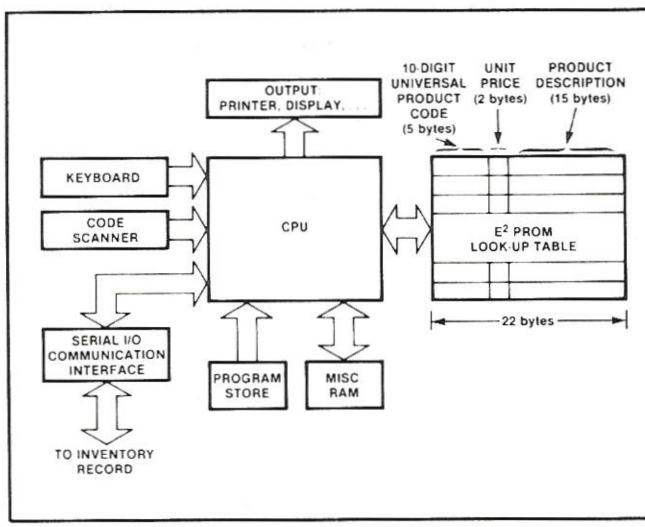


Figure 16. POS Terminal

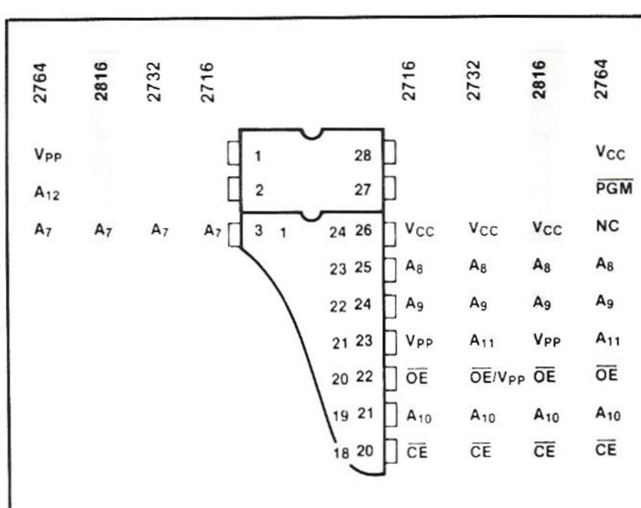


Figure 17. JEDEC 28 Pin Site Byte-Wide Philosophy

Standby Mode

The 2816 has a standby mode which reduces active power dissipation by 55% from 110 mA to 50 mA. The 2816 is placed in the standby mode by applying a TTL high signal to the CE input. When in the standby mode, the outputs are in a high impedance state, independent of the OE input.

Output OR-TIEING

Because 2816s are usually used in larger memory arrays, Intel has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows low power dissipation (by deselecting unused devices), and the removal of bus contention from the system environment.

To most effectively use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded from addresses as the primary device selection function. $\overline{OE}$ (pin 20) should be made a common connection to all devices in system, and connected to the $\overline{RD}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +125°C
All Input or Output Voltages with
Respect to Ground .... +6V to −0.3V
V_{PP}Supply Voltage with Respect to
Ground During Write/Erase .... +22.5V to −0.1V
Maximum Duration of V_{PP} Supply at 22V
During E/W Inhibit .... 24 Hrs.
Maximum Duration of V_{PP} Supply at 22V
During Write/Erase .... 15 ms[8]

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND A.C. OPERATING CONDITIONS DURING READ AND WRITE

	2816	2816-3	2816-4
Temperature Range	0°C-70°C	0°C-70°C	0°C-70°C
V_{CC} Power Supply[9]	5V ± 5%	5V ± 5%	5V ± 5%

D.C. CHARACTERISTICS

READ

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{CC2}	V_{CC} Current (Active)		50	110	mA	OE = CE = V_{IL}
I_{CC1}	V_{CC} Current (Standby)		25	50	mA	CE = V_{IH}
$I_{PP(R)}$	V_{PP} Current (Read)			5	mA	CE = V_{IL}, V_{PP} = 4 to 6
V_{IL}	Input Low Voltage	−0.1		.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA
V_{PP}	Read Voltage	4		6	V	

WRITE

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
V_{PP}	Write/Erase Voltage	20	21	22	V	
$I_{PP(W)}$	V_{PP} Current (Byte Erase/Write)		9	15	mA	CE = V_{IL}
V_{OE}	OE Voltage (Chip Erase)	9		15	V	I_{OE} = 10 μA
$I_{PP(I)}$	V_{PP} Current Inhibit			5	mA	V_{PP} = 22, CE = VIH
$I_{PP(C)}$	V_{PP} Current (Chip Erase)		3	5	mA	

For footnotes see page 13.

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance	5	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance		10	pF	$V_{OUT} = 0V$
$C_{V_{CC}}$	V_{CC} Capacitance		500	pF	$OE = CE = V_{IH}$
$C_{V_{PP}}$	V_{PP} Capacitance		50	pF	$OE = CE = V_{IH}$

A.C. TEST CONDITIONS

Output Load: 1TTL gate and $C_L = 100$ pF
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Level: Input 1V and 2V
Output .8V and 2V

A.C. CHARACTERISTICS

READ

Symbol	Parameter	2816 Limits			2816-3 Limits			2816-4 Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.		
t_{ACC}	Address to Output Delay		200	250		300	350		400	450	ns	$CE = OE = V_{IL}$
t_{CE}	CE to Output Delay		200	250		300	350		400	450	ns	$OE = V_{IL}$
t_{OE}	Output Enable to Output Delay	10		100	10		120	10		150	ns	$CE = V_{IL}$
t_{DF}	Output Enable High to Output Float	0		80	0		100	0		130	ns	$CE = V_{IL}$
t_{OH}	Output Hold from Addresses, CE or OE Whichever Occurred First	0			0			0			ns	$CE = OE = V_{IL}$

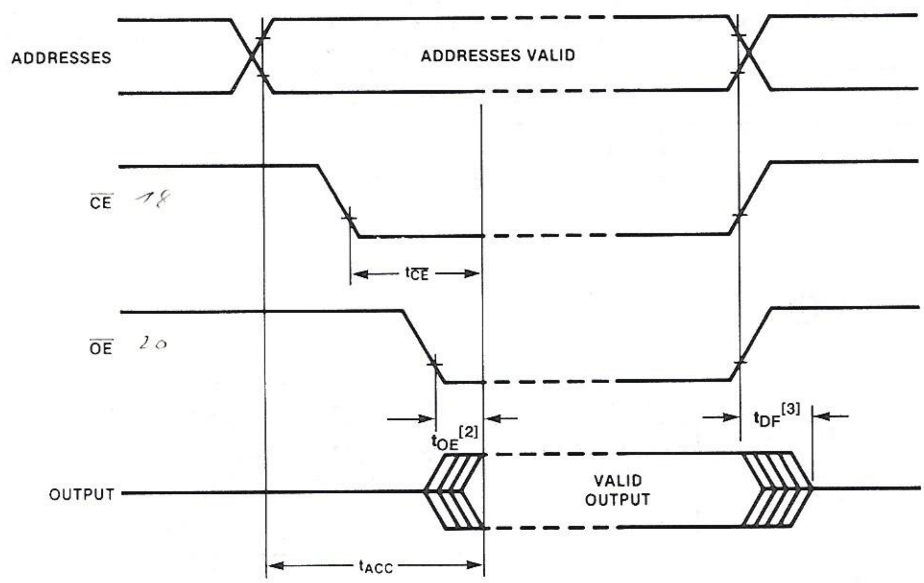
WRITE

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.[1]	Max.		
t_{AS}	Add to V_{PP} Set-Up Time	150			ns	
t_{CS}	CE to V_{PP} Set-Up Time	150			ns	
t_{DS}[10]	Data to V_{PP} Set-Up Time	0			ns	
t_{DH}[10]	Data Hold Time	50			ns	$V_{PP} = 6V$
t_{WP}[8]	Write Pulse Width	9	10	15	ms	
t_{WR}	Write Recovery Time	50			ns	$V_{PP} = 6V$
t_{OS}	Chip Erase Set-Up Time	0			ns	$V_{PP} = 6V$, $V_{OE} = 9V$
t_{OH}	Chip Erase Hold Time	0			ns	$V_{PP} = 6V$, $V_{OE} = 9V$
t_{PRC}	V_{PP} RC Time Constant	450	600	750	μs	
t_{PFT}[7]	V_{PP} Fall Time			100	μs	$V_{PP} = 6V$
t_{BOS}	Byte Erase/Write Set-Up Time	0			ns	$V_{PP} = 6V$
t_{BOH}	Byte Erase/Write Hold Time	0			ns	$V_{PP} = 6V$

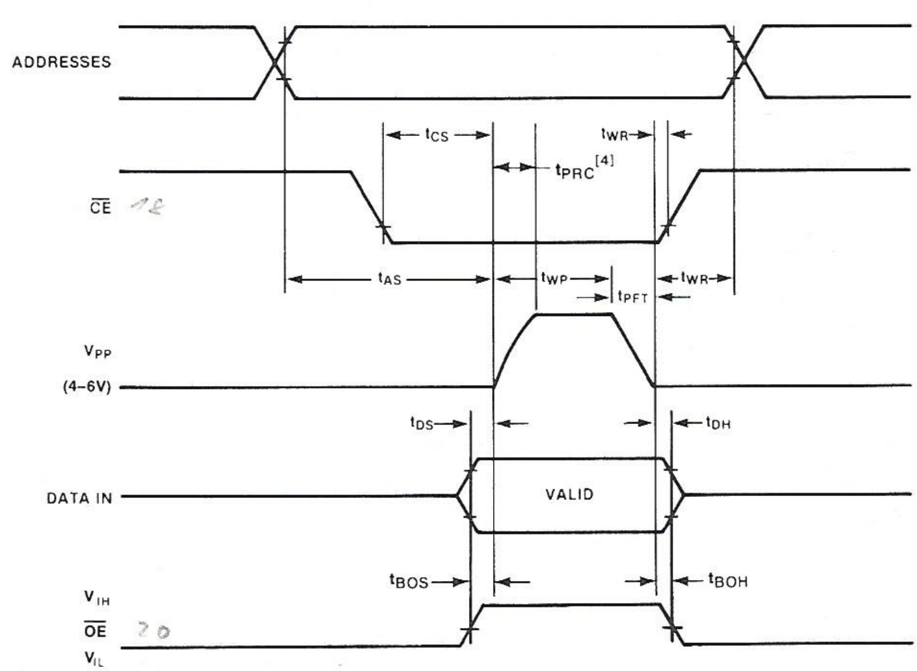
For footnotes see page 13.

WAVEFORMS

READ



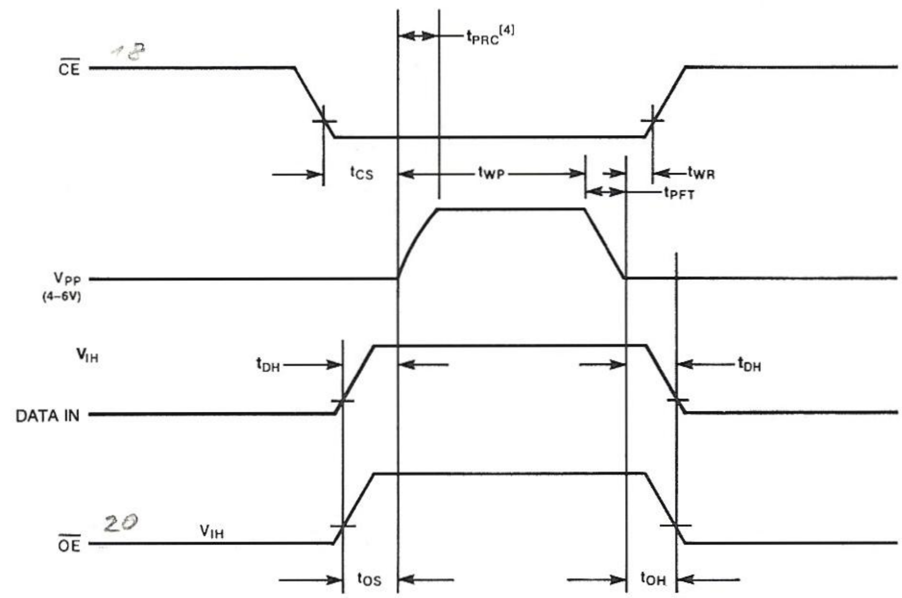
BYTE ERASE[5] OR WRITE



For footnotes see page 13.

WAVEFORMS (Continued)

CHIP ERASE[6]



NOTES:

1. This parameter is only sampled and not 100% tested.
2. OE may be delayed up to 230 ns after falling edge of CE without impact on t_{ACC} for 2816.
3. t_{DF} is specified from OE or CE whichever occurs first.
4. The rising edge of V_{PP} must follow an exponential waveform. That waveform's time constant is specified as t_{PRC}. See Intel's AP-102 for details.
5. Prior to a data write, an erase operation must be performed. For erase, data in = V_{IH}.
6. In the chip erase mode $D_{IN} = V_{IH}$.
7. To allow immediate read verify capability, V_{PP} can be driven low in less than 50 ns. See AP-101 for more information.
8. Adherence to TWP specification is important to device reliability.
9. To prevent spurious device erasure or write, V_{CC} must be applied simultaneously or before 21 volt application of V_{PP}. V_{PP} cannot be driven to 21 volts without previously applying V_{CC}.
10. The data in set up and hold times for chip erase are identical to those specified for byte erase.
11. This switch includes automatic voltage shutdown on power fail.

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Target Spec.

19. Okt. 1979 (IE-1B)

Sep.1, 1978

HITACHI
Semiconductor & Integrated Circuits Div.

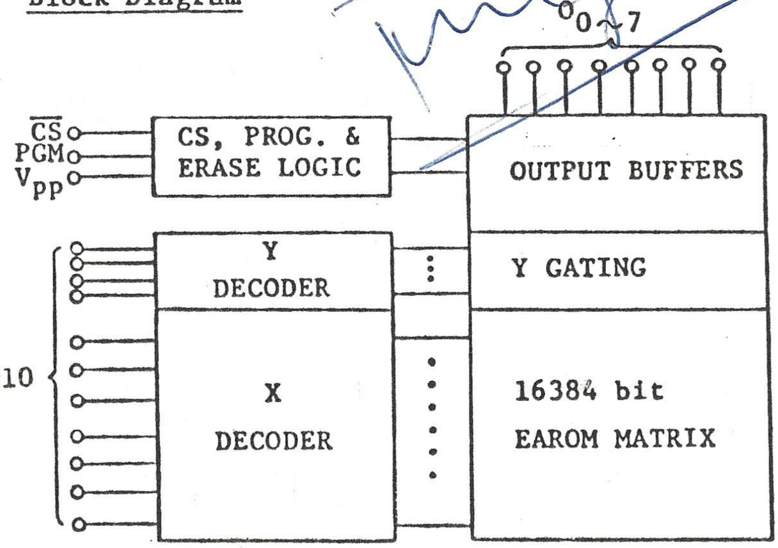
HN48016

2048 word x 8 bit Electrically Erasable and Programmable Read Only Memory

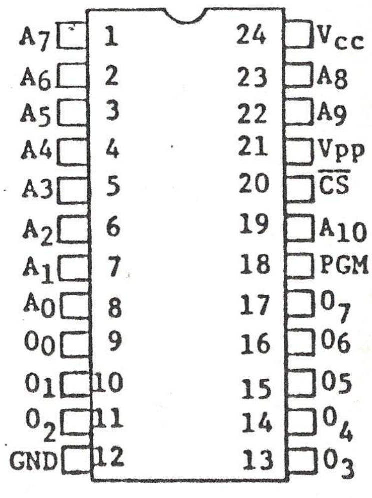
The HN48016 is a 2048 word by 8 bit electrically erasable and programmable ROM's. This device operates from a single 5-volt power supply and features fast single address location programming. All the words are erased by one TTL level pulse. Erasing the bit pattern and programming new pattern can be made within 3 seconds.

- Single Power Supply ----- 5V ± 10%
- Simple Programming -----Program Voltage:+25V DC. Programs with one 0.8 ms pulse
- Electrical Erasing -----Erase Voltage:+25V DC. Erases all words with one 1 sec pulse
- Fully Static -----No clocks required.
- Inputs and Outputs are TTL compatible during read, program and erase modes
- Fully Decoded ----- On-chip address decode
- High Speed -----Access Time 300 ns max.
- Low Power Dessipation -----300 mW max.
- Three State Output -----OR-Tie Capability
- Interchangeable with Intel 2716

Block Diagram



Pin Arrangement



(Top View)

MODE SELECTION

MODE \ PINS	PGM (18)	$\overline{CS}$ (20)	V_{pp} (21)	V_{cc} (24)	OUTPUTS (8~11,13~17)
READ	V_{IL}	V_{IL}	+5	+5	D_{out}
DESELECT	Don't Care	V_{IH}	+5	+5	High Z
PROGRAM	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	Din
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	+5	Dout
ERASE	Pulsed V_{IL} to V_{IH}	V_{IL}	+25	+5	

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

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Absolute Maximum Ratings

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +125°C
All Input or Output Voltages with respect to Ground	-0.3V to +7V
V_{pp} Supply Volgate with respect to Ground	-0.3V to +28V

READ OPERATION

DC and Operating Characteristics

T_A=0°C to 70°C,V_{cc}=+5V ± 10%, V_{pp}=V_{cc} ± 0.6V [1)]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Load Current	I_{LI}	V_{IN}=5.5V			10	μA
Output Leakage Current	I_{LO}	V_{OUT}=5.5V			10	μA
V_{cc} Current	I_{cc}	$\overline{CS}$=V_{IH}		32	50	mA
V_{pp} Current	I_{pp1}	V_{pp}=6.1V		4	7	mA
Input Low Voltage	V_{IL}		-0.1		0.8	V
Input High Voltage	V_{IH}		2.0		V_{cc} +1	V
Output Low Voltage	V_{OL}	I_{OL}=1.6mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=-100μA	2.4			V

NOTE: 1) The tolerance of 0.6V allows the use of a driver circuit for switching the V_{pp} supply pin from V_{cc} in read to 25V for programming.

AC Characteristics

T_A=0°C to 70°C, V_{cc}=5V ± 10%, V_{pp}=V_{cc} ± 0.6V

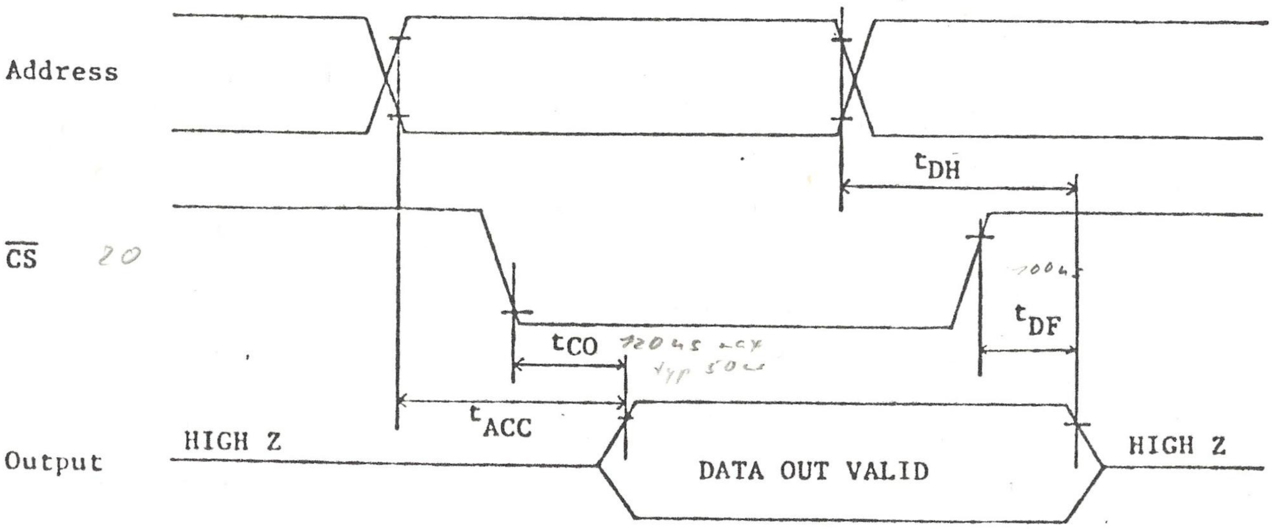
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address to Output Delay	t_{ACC}	PGM=$\overline{CS}$=V_{IL}		170	300	ns
Chip Select to Output Delay	t_{CO}	PGM=V_{IL}		50	120	ns
Chip Deselect to Output Float	t_{DF}		0	40	100	ns
Address to Output Hold	t_{DH}	PGM=$\overline{CS}$=V_{IL}	10			ns

AC Test Conditions;Output Load:1 TTL gate and C_L=100 pF
Input Rise and Fall Times: ≦20 ns
Input Pulse Levels:0.8V to 2.0V
Timing Measurement Reference Level:
Inputs 1V and 1.8V
Outputs 0.4V and 2.4V

Capacitance(T_A=25°C, f=1MHz)

Parameter	Symbol	Conditions	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V		7.5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V		15	pF

Waveforms



PROGRAM OPERATION

DC Programming Characteristics

T_A=25°C ± 5°C, V_{cc}=5V ± 10%, V_{pp}=25V ± 1V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Current(for Any Input)	I_{LI}	V_{IN}=5.5V			10	μA
V_{cc} Supply Current	I_{cc}			32	50	mA
V_{pp} Supply Current	I_{pp2}			5	10	mA
Input Low Level	V_{IL}		-0.1		0.8	V
Input High Level	V_{IH}		2.0		V_{cc} +1	V

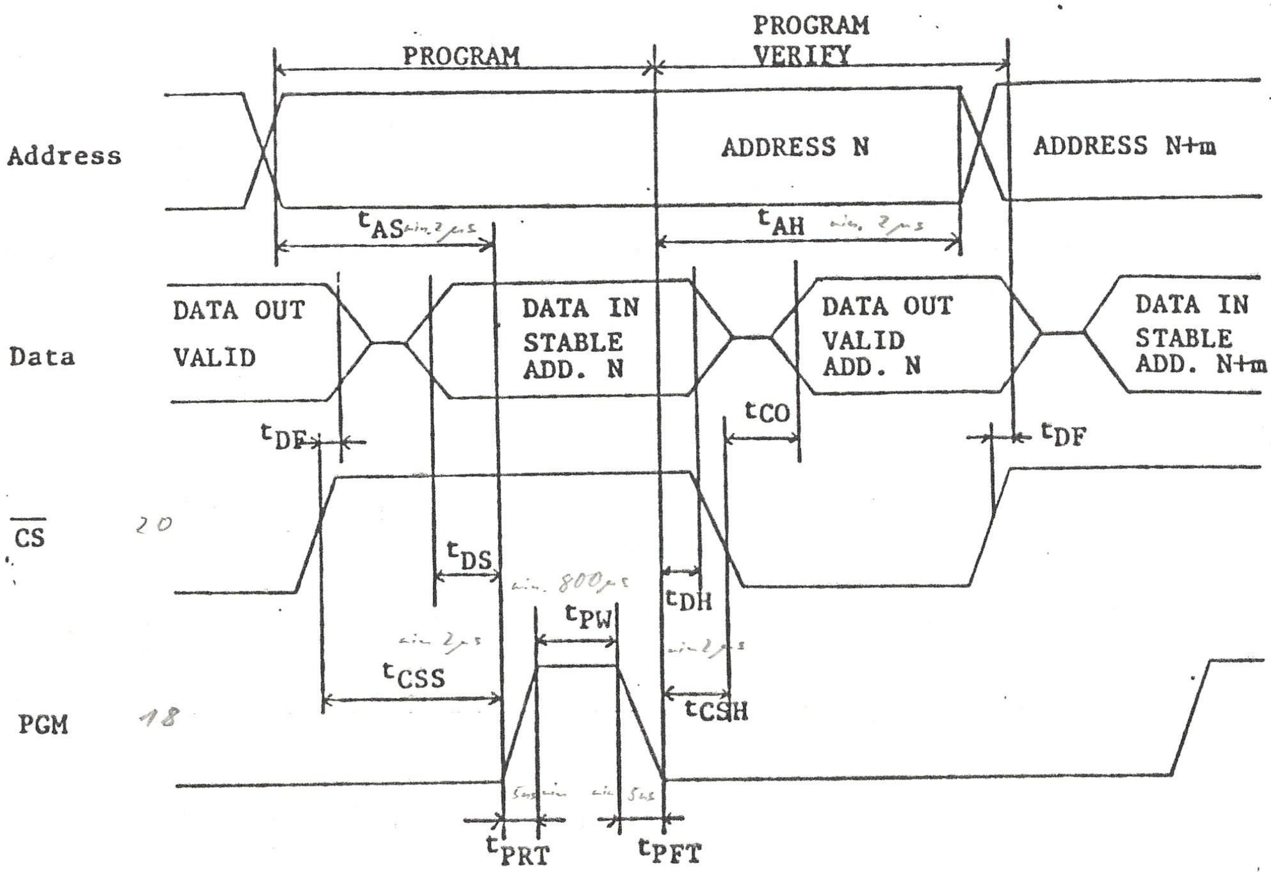
AC Programming Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address Setup Time	t_{AS}		2			μs
$\overline{CS}$ Setup Time	t_{CSS}		2			μs
Data Setup Time	t_{DS}		2			μs
Address Hold Time	t_{AH}		2			μs
$\overline{CS}$ Hold Time	t_{CSH}		2			μs
Data Hold Time	t_{DH}		2			μs
Chip Deselect to Output Float Delay	t_{DF}		0	40	100	ns
Chip Select to Output Delay	t_{CO}			50	120	ns
Program Pulse Width	t_{PW}		800			μs
Program Pulse Rise Time	t_{PRT}		5			ns
Program Pulse Fall Time	t_{PFT}		5			ns

10 ms

AC Test Conditions; V_{cc}:5V ± 10%
V_{pp}:25V ± 1V
Input Rise and Fall Times(10% to 90%) 20 ns
Input Pulse Level:0.8V to 2.0V
Input Timing Reference Level:1V and 1.8V
Output Timing Reference Level:0.4V and 2.4V

Programming Waveforms



ERASE OPERATION

DC Erasing Characteristics

T_A=25°C ±5°C, V_{cc}=5V ± 10%, V_{pp}=25V ±1V

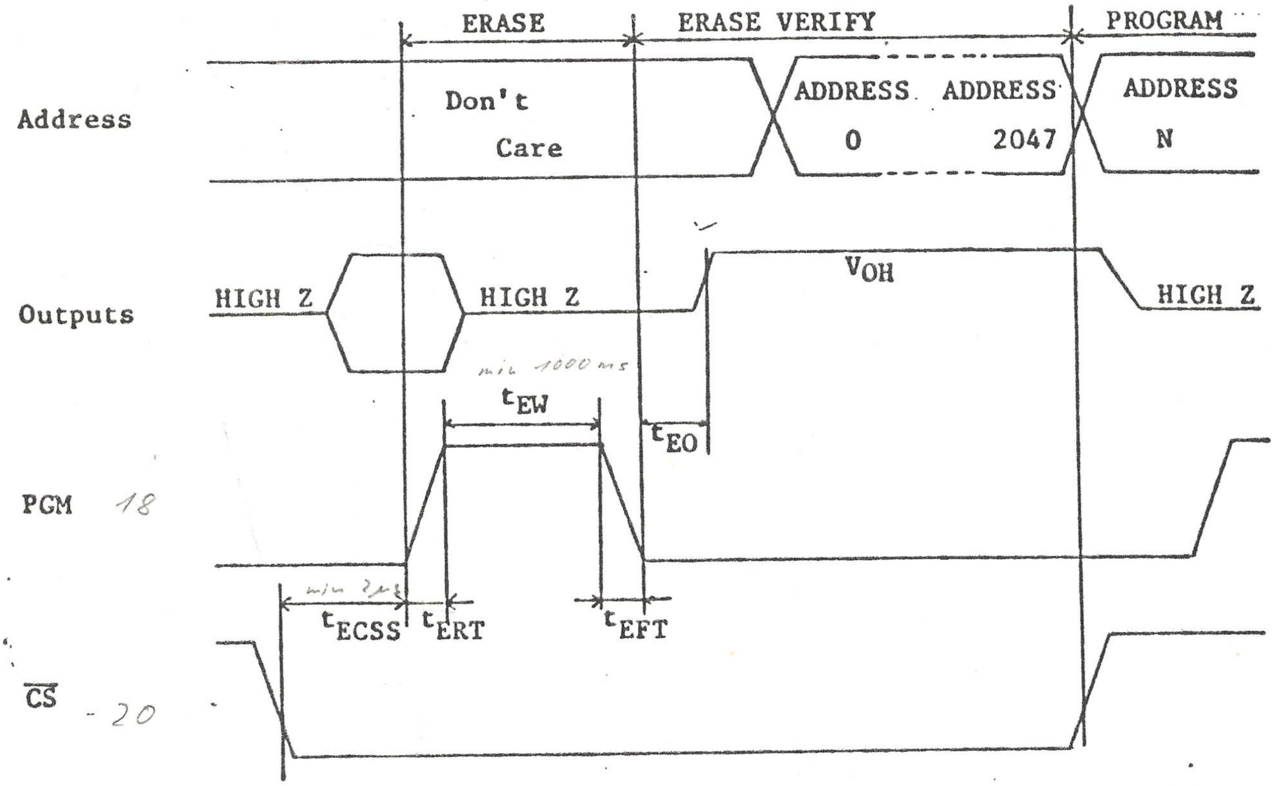
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Current(for Any Input)	I_{LI}	V_{IN}=5.5V			10	μA
V_{cc} Supply Current	I_{cc}			32	50	mA
V_{pp} Supply Current	I_{pp}			5	10	mA
Input Low Level	V_{IL}		-0.1		0.8	V
Input High Level	V_{IH}		2.0		V_{cc} +1	V

AC Erasing Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
$\overline{CS}$ Setup Time	t_{ECSS}		2			μs
PGM to Output Delay	t_{EO}		2			μs
Erase Pulse Width	t_{EW}		1000			ms
Erase Pulse Rise Time	t_{ERT}		5			ns
Erase Pulse Fall Time	t_{EFT}		5			ns

AC Test Conditions; V_{cc}:5V ± 10%
Vpp:25V ± 1V
Input Rise and Fall Times(10% to 90%) 20 ns
Input Pulse Level:0.8V to 2.0v
Input Timing Reference Level:1V and 1.8V
Output Timing Reference Level:0.4V and 2.4V

Erasing Waveforms



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