A Novel Architecture Design & Characterization of CAM Controller IP Core with Replacement Policy

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ABSTRACT

Content Addressable Memory (CAM) is a special purpose Random Access Memory device that can be accessed by searching for data content. This paper describes a novel architecture design and characterization of a reusable soft IP core for CAM controller with sequential replacement policy, so as to improve the match ratio of the CAM memory. The proposed design was modeled using Verilog HDL and also prototyped in Xilinx® SPARTAN family FPGA.The power analysis was done using XPower® analyzer and the hardware test result was obtained by ChipScope® Pro logic analyzer.

1. SCOPE OF THE PROJECT

The CAM controller design described in this paper is a custom general purpose controller. This controller is having a reconfigurable architecture. Replacement policy is an important feature of this controller which can be effectively used to improve the match ratio of the CAM memory. This work is believed to serve as a good benchmark for selecting an optimum controller core for Content Addressable Memory (CAM), so as to improve the match ratio.

2. PROJECT REQUIREMENTS

a. Simulation & Synthesis Tool – Xilinx® ISE 12.1

Simulation and Synthesis is done using Xilinx® ISE 12.1.Xilinx® ISim is a Hardware Description Language (HDL) simulator that enables you to perform functional and timing simulations for VHDL, Verilog and mixed VHDL/Verilog designs. Logic Synthesis is the process of translating an HDL model into a technology-specific gate-level description.

b. Programming Language – Verilog HDL

The programming language used in this project is Verilog HDL. Verilog, standardized as IEEE 1364, is a hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction. It is also used in the verification of analog circuits and mixed-signal circuits.Verilog HDL has evolved as a standard Hardware description language. Verilog HDL

offers many useful features for hardware design and the reason for choosing this standard in this project is given below:-

- ➤ Verilog HDL is a general purpose hardware description language that is easy to learn and easy to use. It is similar in syntax to the C programming language.

- ➤ Verilog HDL allows different levels of abstraction to be mixed in the same model. Thus, a designer can define a hardware model in terms of switches, gates, RTL or behavioural code. Also, a designer needs to learn only one language for stimulus and hierarchical design.

- ➤ Most popular logic synthesis tools support Verilog HDL .This makes it the language of choice for designers.

- ➤ All fabrication vendors provide Verilog HDL libraries for post logic synthesis simulation. Thus, designing a chip in Verilog HDL allow the widest choice of vendors.

- ➤ The programming language Interface (PLI) is a powerful feature that allows the user to write custom C code to interact with the internal data structures of Verilog. Designers can customize a Verilog HDL simulator to their needs with the PLI.

c. CAM core Generator – IP core generator software.

The LogiCORE™ IP Content-Addressable Memory (CAM) core is a fully verified memory unit that uses content matching rather than addresses. The core enables faster data searches as compared to other memory implementations and offers parallel content compares to find a valid address. The width, depth, memory type, and other optional features of the CAM core can be customized using the CORE Generator software

3. INTRODUCTION

A type of memory commonly used in many types of switching circuits is a Content Addressable Memory (CAM).Compared to a Random Access memory (RAM), a Content Addressable Memory (CAM) has a unique method of accessing data words within the memory. In a Random Access memory, during a read operation an address is supplied that uniquely identifies one location within the memory. The memory responds with a data word stored in the

addressed memory location. The Content Addressable memory is a special purpose Random Access Memory device that can be accessed by searching for data content. For this purpose, it is addressed by associating the input data, simultaneously with all the stored words and produces output signals to indicate the match condition between the input data and the stored words. This operation is referred to as association or interrogation and this type of memory is also known as Associative memory [2].

In this era of fast processors and processors with many cores, there is a requirement for faster and bigger memories. But today the speed of memories is not able to match up with the speed of processors. So there is the need for fast memory controllers. Memory controller is used to control the memory through interface. The controller is expected to synchronize the data transfer between the processor on one side of the controller and the memory on the other side. To achieve this, the controller has to accept the requests from the processor side and convert them to a form suitable to the memory and execute the requests [7].

Replacement policies determine which data item(s) should be deleted from the memory when the free space is insufficient for accommodating an item [6].It is one of the factors that determine the hit rate .There are different types of cache replacement policies [4], [5], [6].

In this paper a novel architecture design of a CAM Controller core with sequential replacement policy is described [4]. Sequential replacement policy is used to improve the "match ratio" of the CAM memory and it consumes only little power [4]. The CAM memory targeted in this design is Content-Addressable Memory version 6.1 by Xilinx® [1].The CAM core is a fully verified memory unit that uses content matching rather than addresses. The core enables faster data searches as compared to other memory implementations and offers parallel content compares to find a valid address. The width, depth, memory type and other optional features of the CAM core can be customized to fit wide variety of applications. The CAM used here is 256x16 and the memory type is Block RAM. Since the memory type is Block RAM, the write operation takes two clock cycles latency and read operation has one clock cycle latency [1].The match address type is binary encoded .In the CAM memory there is a priority encoder, which is used to select the match address with highest priority. It can be either lowest or highest resolution. And here lowest match address resolution is selected. Memory initialization is done by adding a table that contains the initial contents of the memory [1].

4. PRINCIPLE OF OPERATION

The various stages of the controller can be explained by a Finite State Machine (FSM), as shown in Figure 1.
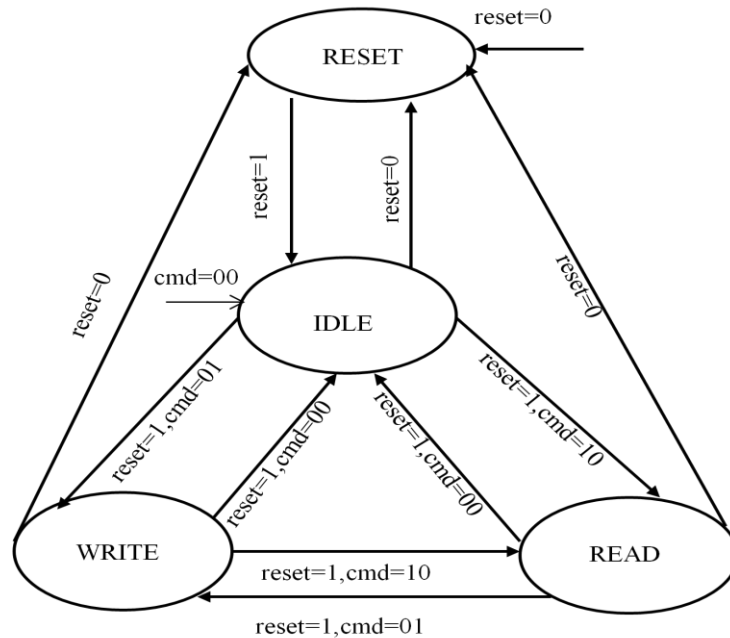

Figure 1: Finite State Machine for Controller

The controller typically has four stages (i) RESET (ii) IDLE (iii) WRITE (iv) READ. The reset is an active low signal and when reset the entire controller and the memory will be in the RESET state. When the reset is active high the controller will be in the IDLE state. When we give the cmd (command) "00" when the controller is in the IDLE state then the controller will remain in the IDLE state itself. When we give the cmd "01" the controller will be in the WRITE state. We can give the address location and the data input to write to the specified location in the memory. When the cmd is "10" the controller will be in the READ state and we can give the data input to perform search operation to determine whether the data is present in a location within the memory. If the data is present in any of the memory location, then the corresponding address where the data resides will be present at the output. The output signals to indicate the match condition will also be asserted.

If the data is not present in any of the memory locations, then the replacement block simply increments an address counter sequentially to points to the location of the new entry [4].The search input data will be written to the memory location pointed by the address counter

and the corresponding address will be present at the output. The controller is responsible for migrating the CAM through all the states as explained in [1].

5. DESIGN METHODOLOGY

A. INTRODUCTION

The CAM controller is designed to work with Xilinx® CAM version 6.1.It has a user interface on one side and the memory on the other side. The controller architecture consists of Control unit, Data path & Address unit, a built in Replacement block to improve the match ratio of the memory and a Select logic.

B. BLOCK DIAGRAM

The CAM controller is used to control the CAM memory through interface. The block diagram of the controller with sequential replacement policy consists of Control unit, Data path & Address unit and a Replacement block. The block diagram for the controller along with the CAM memory is shown in Figure 2.
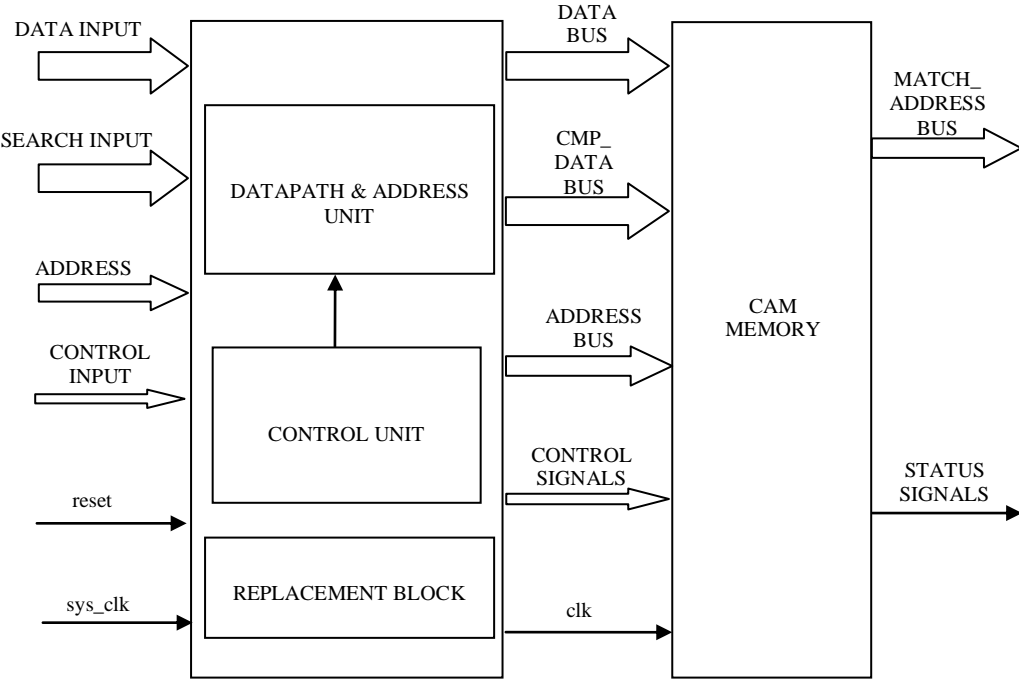

Figure 2: Block Diagram

The controller consists of Control unit, Data path & Address unit, Replacement block and a Select logic. The CONTROL SIGNALS from the control unit are given to the memory and also to the Data path & Address unit. The DATA INPUT and the SEARCH INPUT to the controller is 16 bit. The ADDRESS is 8 bit. The CONTROL INPUT is the user command to the controller and it is of 2 bit. The sys_clk (system clock) and reset signal is also given to the controller. The DATA BUS and CMP_DATA_BUS from the controller to the memory is 16 bit. The ADDRESS BUS is 8 bit. The control signals to the memory and the Data path & Address unit are "en" (enable) and "we" (write enable) signals.

The MATCH_ADDRESS BUS indicates the address that matches the contents of the CMP_DATA_BUS.Status signals are "busy", "match", "single_match" and "multiple_match".The "busy" signal will remain asserted during a write operation and will be low during read operation. The "match" signal will be asserted when the data on the CMP_DATA_BUS matches data in one or more locations in the CAM. When more than one match is present in the CAM "multiple_match" signal is asserted and when there is only one match "single_match" signal is asserted. During read operation when the data is not present in any of the memory locations, then the "match" signal will be low. At that time the replacement block will carry out the replacement of the data in a sequential manner starting from the first location.

C. PIN DESCRIPTION

The Input/output diagram for the controller is shown in Figure 3.The output ports from the controller are given as input ports to the memory.

All the pins in the Input/output diagram of the controller are described in Table I. The direction and the description of the pins are also given.
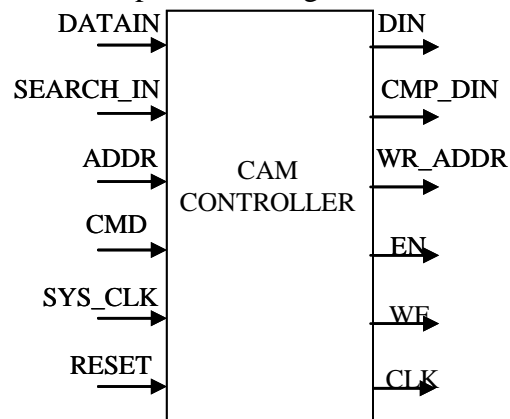

Figure 3: Input/output diagram for
the controller

The pin description for the controller is given below

Table I: Pin description

PORT NAME	DIRECTION	DESCRIPTION
SYS_CLK	Input	All the operations are synchronous to the rising-edge of the system clock input
RESET	Input	This is used to reset the controller and the memory
DATAIN	Input	This is the 16 bit data given to the controller during write operation
SEARCH_IN	Input	This is the 16 bit data given to the controller during read operation
CMD	Input	This is the 2 bit command signal given to perform various operations.
ADDR	Input	This is the 8 bit address given to the controller during write operation
DIN	Output	Data to be written to the CAM ,by the controller during write operation
CMP_DIN	Output	Data to look up from the CAM during read operation
WR_ADDR	Output	The location that the data on DATA BUS will be written into the CAM
EN	Output	Control signal used to enable both write and read operation
WE	Output	Control signal used to enable transfer of data into CAM from the DATA BUS. During write operation "WE" is high and during read operation it is low
CLK	Output	All the operations are synchronous to the rising-edge of the clock input to the memory

D. PROPOSED CONTROLLER ARCHITECTURE

The complete architecture of the controller along with the memory is shown in Figure 4.The CAM controller is used to control the CAM memory through interface. The replacement block within the controller is used to improve the "match ratio" of the memory when the free space is insufficient for accommodating a data item. Each and every unit given in Figure 4 is explained below.

1. Control Unit

This unit is responsible for generating the control signals to the memory and the Address & Data path unit.   The control signals generated by the control unit are "en" (enable) and "we" (write enable).The command input "cmd" is given to the control unit by the processor. As explained earlier the controller has a transition through four states. When the given command input is "cmd=00" controller will be in the IDLE state. At this time en=0 and we=0.The write and read operation can be performed only if the "en" signal is high. The command input for write operation is "cmd=01". At this time en=1 and we=1 and controller is in the WRITE state. The command input for read operation is "cmd=10" .At this time en=1 and we=0 and the controller is in the READ state.

2. Data path & Address Unit

This unit of the controller consists of Data register, Comparand register and Address register. The Data register is for the storage of input data to the controller, during write operation. At the rising edge of the system clock the data at the DATA INPUT BUS will be available at the DATA BUS. At this time the control signals en=1 and we=1. This register is of 16 bit and a parallel in parallel out (PIPO) register can be used. The Comparand register is meant for the storage of data during a read operation. At the positive edge of the system clock the data at the SEARCH INPUT BUS will be available at the CMP_DATA BUS. At this time en=1 and we=0.Comparand register used here is a 16 bit PIPO.The Address register is used during write

operation and it is an 8 bit PIPO register. The input address will be available at the ADDRESS BUS during the rising edge of the system clock and at this time en=1 and we=1.The "match_addr" is the CAM address where matching data resides. The "match"signal indicates that at least one location in the CAM contains the same data as the DATA BUS. The "single_match" signal indicates the existence of matching data in one location of the CAM. The "multiple_match" signal indicates the existence of matching data in more than one locations of the CAM. The "busy" signal indicates that a write operation is currently being executed.

3. Replacement Block

This unit is responsible for determining which data item(s) should be deleted from the memory when the free space is insufficient for accommodating a data item. It is an important factor that improves the match ratio of the memory. A sequential replacement policy is used here.This type of replacement policy consumes only little power [4]. When the controller is in the read state the data at the SEARCH INPUT BUS will be available at the CMP_DATA BUS .The memory locations will be searched simultaneously for the data. If the data is not present in any of the memory locations then the "match" signal will be low. Then the replacement block will be active. The replacement block simply increments an address counter sequentially to points to the location of the new entry [4]. Then the search input data will be written to that location. To perform this replacement the "en" and the "we" signal should be high.

4. Select Logic

This unit is responsible for selecting either the outputs from the replacement block or the outputs from the control unit and data path & address unit. The outputs from the replacement block are selected if the data that is searched for is not present in any of the memory locations. At this time the "S0" signal will be high. The outputs from the control unit and data path & address unit will be selected when the data that is searched for is present in any of the memory locations and at this time the "S0 signal will be low.
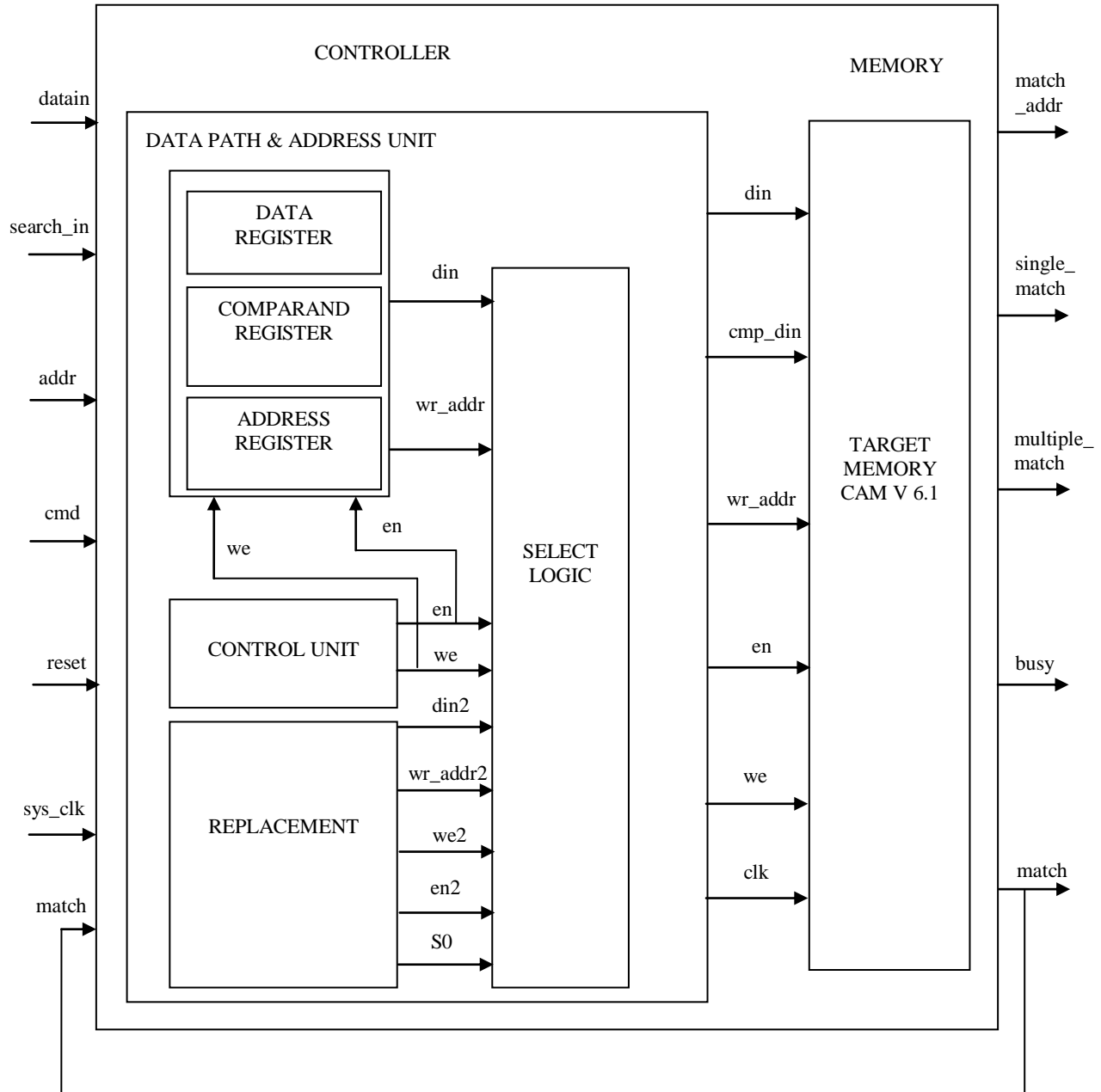
Figure 4: Controller test environment architecture

6. IMPLEMENTATION AND RESULTS

The design program for the controller with replacement policy for the CAM v 6.1 of Xilinx® is simulated functionally verified and synthesized using Xilinx ISE® design suite. The target device is SPARTAN® 3AN FPGA by Xilinx® [3].

a. Simulation Results

The simulation result for the controller along with the memory is shown in Figure 5.

Figure 5: Simulation result

b. Synthesis Result

Table II shows the power analysis done and Table III shows the device utilization result.

Table II: Power analysis report

Table III: Device utilization report

LOGIC UTILIZATION	USED	AVAILABLE
Total Number Slice Registers	664	11,776
Number Used as Flip Flops	663	
Number Used as Latches	1	
Number of 4 input LUTs	2,025	11,776
Number of occupied Slices	1,317	5,888
Number of Slices containing only related logic	1,317	1,317
Number of Slices containing unrelated logic	0	1,309
Total Number of 4 input LUTs	2,080	11,776
Number used as logic	1,666	
Number used as route-thru	55	
Number used for 32x1 RAMs	256	
Number used as shift registers	103	
Number of bonded IOBs	18	372
Number of BUFGMUXS	2	24
Number of BSCANS	1	1
Number of BSCAN_SPARTAN3As	1	1
Number of RAMB16BWEs	17	20
Number of RAM macros	20	
Average Fan-out of Non-clock Nets	3.38	

The Hardware test result was obtained using Chip Scope® Pro logic analyzer and the logic analysis for reset, idle, write, read and replacement operation is shown in Figure 7, Figure 8,Figure 9 ,Figure 10 and Figure 11 respectively. In Figure 7 and in Figure 8 all the signals are low. In Figure 9, the "busy" signal is asserted in order to show that a write operation is currently being executing. In Figure 10 "busy" signal is low in order to show that it is a read operation. In this case a data which is previously written once is given and hence "match" and "single_match" signal is high and "multiple_match" signal is low. The address where the data is written is present at the

"match_addr". In Figure 11 the replacement operation to the zeroth location is shown and hence the "match_addr" is 8'b00000000.
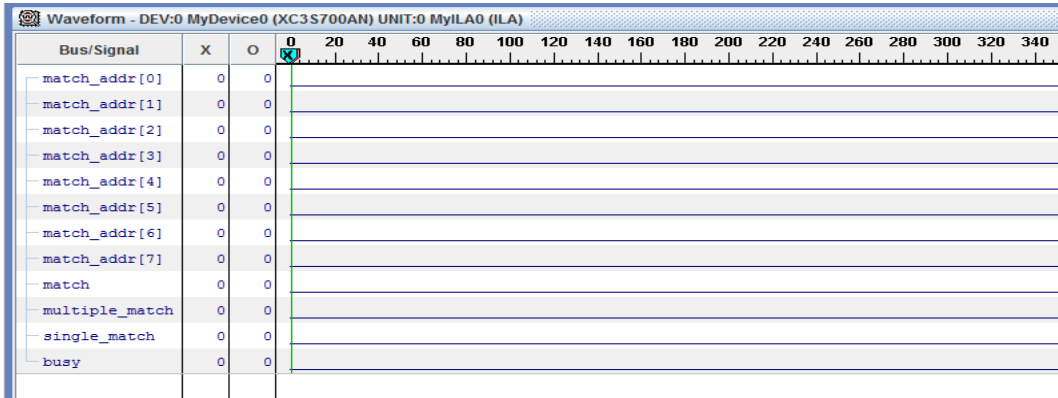

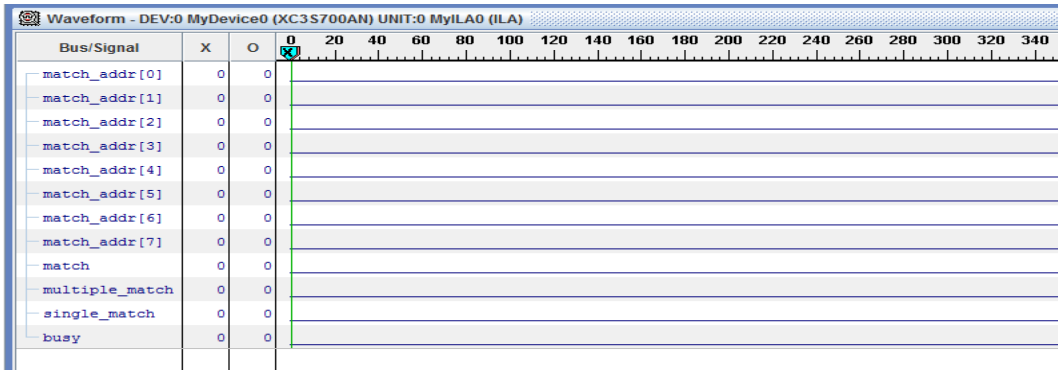Figure 7: Hardware test result for reset operation

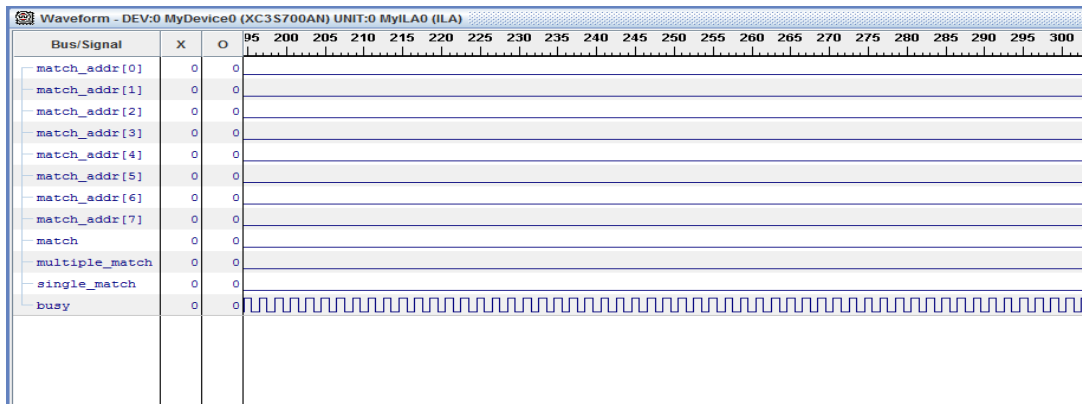Figure 8: Hardware test result for idle operation
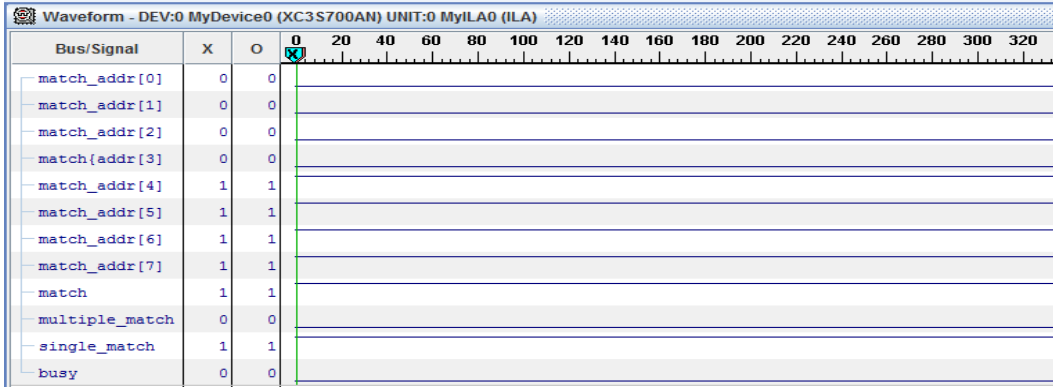

Figure 9: Hardware test result for write operation

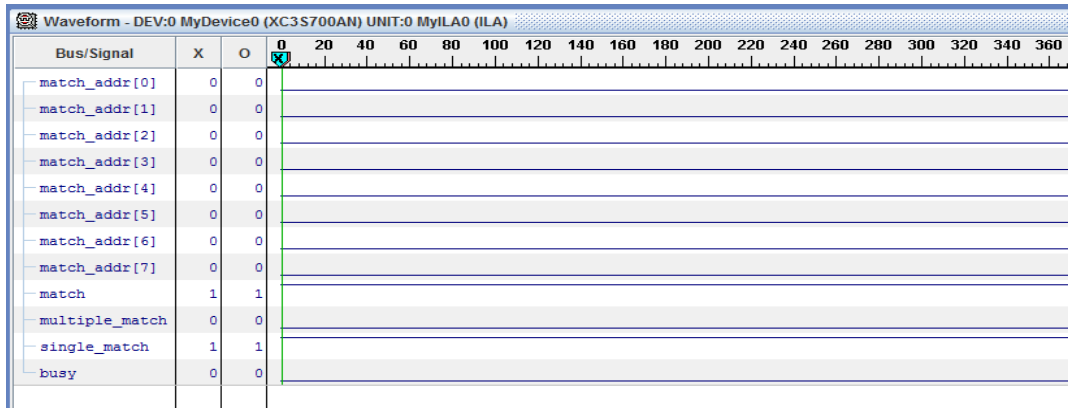Figure 10: Hardware test result for read operation

Figure 11: Hardware test result for replacement operation

7. CONCLUSION

Content Addressable Memory (CAM) is a special purpose Random Access Memory (RAM) device that can be accessed by searching for data content. The architecture of a custom controller with Sequential replacement Policy for Content Addressable Memory version 6.1 of Xilinx® was designed,prototyped and characterized for resourse utilization and power consumption. The controller serves as the best reliable interface to the memory. This work is believed to serve as a good bench mark for selecting an optimum controller core for the CAM memory to improve the match ratio of the memory. It can be easily modified for different system design requirements. The proposed design has been tested by implementing the design on SPARTAN 3AN FPGA board which uses XC3S700ANdevice.

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