I/O Techniques

EVALUATION SHEET

1. The five steps of a Programmed Data Transfer and five definitions are given below. Match each step with its definition. Then, in the column labeled Chronological Order, write a 1 next to the first step to be completed, a 2 next to the second step, etc., until the last step is reached.

Step	Definition	Chronological Order
I/O operation	c	3
Process Recycle	e	5
Conditional Loop	b	2
Ready Test	d	1
Ready Flag Reset	a	4

Definitions

a. Sets to 0 immediately after the INPUT instruction has been exhausted.

b. Checks condition of ready flag to deterine whether the program proceeds to the next step or re-executes the test instruction.

c. Performed only after the ready flag is 1.

d. Necessary because the CPU is much faster than peripheral devices.

e. If the I/O operation is to be immediately repeated, the program loops back to the test instruction to wait until the device is ready again.

2. The five steps of a Program Interrupt Data Transfer and five definitions are given below. Match each step with its definition. Then, in the column labeled Chronological Order, write a 1 next to the first step to be completed, a 2 next to the second, etc., until the last step is reached.

Step	Definition	Chronological Order
Register Restored	d	4
Register Saved	a	2
Normal Execution Resumed	e	5
Program Interrupted	c	1
Device Handler Executed	b	3

Definitions

a. Current program data is put aside in memory so that the CPU registers may be used during the data transfer.

b. CPU goes to the interrupt vector to obtain address information, then moves on to the specified address and begins executing instructions.

c. CPU receives a signal on the I/O bus from some device interface.

d. CPU registers returned to their status at the time of the program interrupt.

e. CPU picks up at the point where it was interrupted.

3. Indicate whether each of these statements refers to the polling method (P) or the multiple interrupt levels method (M) of establishing device priorities by writing the correct letter in the space provided.

Statement	P or M
Implemented by hardware via I/O bus.	M
Involves more costly hardware than the other method.	M
Less flexible if priorities are to be changed.	M
Easily changed if priorities require it because priority structure exits as a table.	P
Implemented by software via the device handler.	P
More efficient during execution because it is not necessary to search for the identity of the interrupting device.	M
Less efficient during execution because it requires the executing program to be interrupted before priority is determined.	P
Services an interrupt request by testing each peripheral device until the initiating device is found.	P

4. The seven steps of a DMA Data Transfer and seven definitions are given below. Match each step with its definition. Then, in the column labeled Chronological Order, write a 1 next to the first step to be completed, a 2 next to the second step, etc.

Step	Definition	Chronological Order
Test Completion	e	6
Steal Memory Control	g	3
Program Initiates Transfer	b	1
Signal Completion	a	7
Test Device Readiness	c	2
Update Control Parameters	f	5
Transfer One Word	d	4

Definitions

a. Interface informs the CPU that the transfer has been completed and the device is free.

b. Only step *not* performed by the interface.

c. Interface performs essentially the same check as described for Programmed Data Transfers.

d. One unit of information is moved between the memory and the interface device.

e. Interface checks to determine if all words have been transferred.

f. Current address and word count updated to reflect the transfer of a word.

g. CPU cannot utilize memory, only the interface can.

5. The table below compares the three I/O techniques discussed in this module. Complete the table by writing the correct letters in the spaces provided. (Note that several answers require two letters; a letter may be used more than once.)

Criterion	DMA		Programmed Data Transfers		Program Interrupts	
Advantages	b		c		a	d
Disadvantages	e	g	h	f	e	f
Transfer initiated by	j		j		i	
Transfer controlled by	i		j		j	

Advantages

a. Allows priorities to be established.
b. Is an efficient way to transfer large data blocks.
c. Allows for simple hardware interfaces.
d. CPU does not wait for other devices.

Disadvantages

e. Hardware is expensive.
f. Not efficient for large data blocks.
g. Not efficient for small amounts of data.
h. Wastes CPU time.

Initiation/Control

i. Hardware.
j. Software.