



IEEE

GRID.pdf

September 2005

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Chapter Meetings and Events

- SCV-LEOS - 9/6 | **Silicon Photonics: Opportunity, Apps & Recent Results** - low cost opto-electronic solutions for applications from telecommunications to chip-to-chip interconnects ... [\[more\]](#)
- SCV-IM - 9/7 | **Introduction to the Stanford Nanofabrication Facility, with Research Examples** - an NSF Center with a variety of semiconductor processing equipment open to external use ... [\[more\]](#)
- SCV-MTT - 9/8 | **Load Pull Measurements for Device Characterization** - challenges, interactions, isolation, and calibration ... [\[more\]](#)
- SCV-CPMT - 9/14 | **Kirkendall Voids in Pb-Free Solder Joints** - reliability effects of the impact/shock strength of solder joints .. [\[more\]](#)
- OEB-IAS - 9/15 | **Power System and Equipment Grounding and Personnel Protection** - plus bonding for lightning protection ... [\[more\]](#)
- SCV-CNSV - 9/20 | **Silicon Valley: The BioTransformation of the Valley and Opportunities for Engineers** - an overview of the local biomedical industry and the Biomedical Wave ... [\[more\]](#)
- SCV-Mag - 9/20 | **Recording Performance of Discrete-Track Media** - patterned magnetic disk using nano-imprint lithography . [\[more\]](#)
- SF-Comm - 9/20 | **Technology and Policy Roundtable** - SBC Addresses IPTV, Fiber, Triple Play ... [\[more\]](#)
- SCV-EMB - 9/21 | **Computer-aided Detection in Diagnostic Imaging** - An overview for medical imaging and diagnosis... [\[more\]](#)
- SCV-ED+SSC - 9/21 | **An Overview of MOSFET Device Behavior and Modeling for Mixed-signal/RF IC Design** - device characteristics and behavior at high frequency ... [\[more\]](#)
- SF-GOLD - 9/21 | **Happy Hour With Billiards @ Jillian's** - 'Grads of Last Decade' celebrate in downtown SF (all invited) ... [\[more\]](#)
- SCV-CPMT - 9/22 | **Robert Noyce: The Man Behind the μ chip** - author of the new biography on Noyce discusses his impact ... [\[more\]](#)
- SF-IAS - 9/27 | **Overview: IEEE Standard 1015 ("Blue Book")** - Applying low-voltage circuit breakers in Industrial Systems ... [\[more\]](#)
- SCV-Rel - 9/28 | **Built-In Soft Error Resilience for Robust System Design** - radiation-induced logic soft errors ... [\[more\]](#)
- OEB-IAS - 10/1 | **Full-day Seminar: 2004 California Electrical Code** - for Electrical Facility Engrs and Design Consultants ... [\[more\]](#)
- SF-PES - 10/4 | **Annual Banquet: The Future of California Energy** - re-examining reliability standards and the adequacy and security of system infrastructure ... [\[more\]](#)
- SCV-CPMT - 10/12 | **Imprint Patterning: An Alternative Circuit Fabrication Process** - ... a microreplication operation [\[more\]](#)
- OEB-IAS - 10/13 | **AC Control Power and Digital Protective Relays: Avoiding the Pitfalls** - issues and techniques for digital relays requiring a separate control power source ... [\[more\]](#)
- SCV-CPMT - 10/27 | **Drop Testing of Components in Portable Applications** - portable devices (cell phones, PDAs) are more likely to be dropped than affected by changes in thermal condition ... [\[more\]](#)

Upcoming Conferences in the Bay Area

- Sept 12-15: **Int'l Symposium on Semiconductor Manufacturing** - San Jose Fairmont - Workshops, Sessions, keynotes, panel [\[more\]](#)
- Sept 22-23: **Antenna Systems and Short-Range Wireless Conferences**, Held at Santa Clara Marriott for semiconductor device manufacturers, suppliers [\[more\]](#)
- Oct 24-27: **GSPx'05: Pervasive Signal Processing Conference and Expo**, at Santa Clara Convention Center; **GRID** & Early-bird discounts through September 15th [\[more\]](#)
- Call for Papers: ISQED'06
Int'l Symposium on Quality Electronic Design
San Jose ... Manuscripts due Oct. 26th [\[more\]](#)

Online graduate programs
MS-EE, MS-Telecom, Certificates in Networking Polytechnic University [\[more\]](#)
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- Full-day Seminar: 2004 California Electrical Code** - October 1 ... for Facility Engrs, Design Consultants [\[more\]](#)
- Full-day: Consultants' Business Seminar** - Oct. 22 ... Learn about Engineering Consulting as a career [\[more\]](#)

- Professional Skills Courses** from EMS, CPMT, ETA:
- Creative Problem Solving**
Sept 14 at LSI Logic, Milpitas [\[more\]](#)
- Managing Time & Multiple Priorities**
Sept 15 at Exar Corp, Fremont (half-day) [\[more\]](#)
- Getting Things Done Across Organizational Borders**
Sept 20 at BEA Systems, San Jose [\[more\]](#)
- Clear Business, Technical, and E-mail Writing**
Oct 6 at Cypress Semiconductor, San Jose [\[more\]](#)
- Leadership Skills for Engineers**
Oct 19 at LSI Logic, Milpitas [\[more\]](#)

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IEEE GRID

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IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

IEEE GRID is published as the **GRID** Online Edition residing at www.e-GRID.net, and in a handy printable **GRID.pdf** edition, and also as the **e-GRID** sent by email twice each month to more than 24,000 Bay Area members and other professionals.



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From the editor . . .

Fall is a time of new beginnings. The children head off to the next grade in school, and our IEEE Chapters gear up their programs for the post-vacation period after a quiet summer. Note how the number of Chapter meetings has mushroomed in the last month!!

Sometimes, in our careers, there are opportunities for “new beginnings.” Well, maybe not quite that – more like chances to try a new direction, or make a change to a different or leading-edge field.

There are several great chances to explore potential changes in your own career, at several autumn seminars. The Oakland-East Bay Industry Applications chapter has a one-day event to bring power engineers up-to-date on the California Electrical Code, on October 1st. And our Consultants’ Network of Silicon Valley has a Saturday seminar that will let the non-consultant (eg, an under-employed or unemployed engineer) explore ways to become a full-time consultant – how to plan it, what to avoid, etc.

Have you considered using your current knowledge and experience to branch out into the bio-engineering and bio-medical fields? That’s the next wave, according to the CNSV’s speaker on September 20th. See page 13 for a summary – plan to attend, if you’d like to position yourself in the forefront of this re-invention of Silicon Valley.

The charter of the GRID.pdf Magazine is to help you network with your peers (that’s why our domain ends in “.net”). We are your Networking Partner – finding chances for you to learn about new and exciting technologies (and other opportunities) and to discuss them with speakers and Chapter leaders who are already involved. In the current economic climate, you can never do too much networking

Paul Wesling editor@e-grid.net

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: www.e-GRID.net

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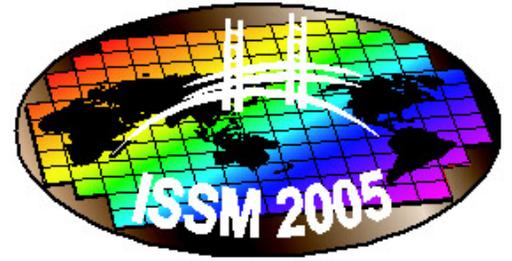
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www.e-grid.net/docs/marketplace-flyer.pdf

ISSM'05 International Symposium on Semiconductor Manufacturing

- Fairmont Hotel, San Jose, CA USA
- Workshops: Monday, September 12
- Sessions: Tuesday – Thursday, September 13-15



The 14th International Symposium on Semiconductor Manufacturing (ISSM) will be held Tuesday, September 13 through Thursday, September 15 at the San Jose Fairmont Hotel. ISSM is the largest world-wide forum specifically designed for semiconductor device manufacturers and suppliers.

This year's event covers timely and important topics: – **Factory Design** – **Manufacturing Strategy and Structure** – **Ultra Clean Technology** – **Process and Metrology Equipment** – **Manufacturing Control and Execution** – **Process Materials Optimization** – **Environment, Safety & Health** – **Robust Engineering** – **Advanced Backend Processing** – **Process Control and Monitoring** – **Yield Enhancement** – **Interactive Poster Session** – and more

Keynote presenters for 2005 include:

- Peter Chang, Vice Chairman, UMC
- Gilles Delfassy, Senior VP of Wireless, TI
- Brian Halla, Chairman/CEO, National Semi
- Tetsuro Higashi, Chairman/CEO, Tokyo Electron
- W.S. Lee, Senior VP of SRAM Flash PA, Samsung
- Mike Polcari, Pres/CEO, International Sematech

Panel: Semiconductors & Semi-Equipment – The Next Opportunity

...debating important issues in our industry.

Two educational workshops will precede the conference on Monday, September 12:

- **Conjoint Design for Manufacturing (DFM) and Advanced Process Control (APC) Strategies for Yield at 65nm and Beyond** (morning)
- **Impact on Manufacturing of Introducing New Materials in IC Production** (afternoon)

Created more than a decade ago by leading corporate executives, ISSM places an emphasis on sharing industrial experiences, technical solutions and opinions on the advancement of manufacturing science. ISSM has developed into one of the most respected and well-attended conferences in the industry. Now celebrating its fourteenth anniversary, ISSM has a stellar conference planned for 2005.



As an international conference, ISSM seeks the best talent from around the world, this year from 77 companies, universities and technical consortia representing 15 countries. Conference presenters include manufacturing professionals, engineers and managers from semiconductor, equipment and materials companies, as well as academic experts from universities and research organizations. Thus, attendees are exposed to the latest technical information.

Recognizing that manufacturing expertise is a cornerstone to corporate success, ISSM places a high priority on relevance, significance and applicability to wafer fabrication. Additionally, plenary presentations provide opportunities for presenting broad visions and outlining key challenges facing the industry.

General information, online conference registration and hotel information is available on the ISSM web site:

www.issm.com

For assistance, contact Drue Hulmer at ISSM, c/o Maritz Travel Co, 1777 Botelho Dr., Suite 100, Walnut Creek, CA 94596 USA

Phone: 925-287-5221, e-mail issm2005@maritz.com

There are numerous parking lots in the area, most with a daily rate of \$16. Parking in most public lots and on the street is free after 6:00 pm.

ISSM is sponsored by the IEEE (Electron Devices Society and Components, Packaging and Manufacturing Technology Society), the Society of Applied Physics of Japan (JSAP), and Semiconductor Equipment & Materials International (SEMI).

31st International Symposium for Testing and Failure Analysis

November 6-10, 2005 • San Jose, CA USA

Tutorials: Sunday & Monday, Nov 6-7
Sessions: Tuesday-Thursday, Nov 8-10
Exposition: Tuesday-Wednesday, Nov 8-9

Held this year for the first time at the San Jose Convention Center, ISTFA'05 combines technical sessions, tutorials, an exhibition, and user group meetings with a focus on making the full experience a strong benefit for the attendee. The limited number of selected, high-quality papers only requires two tracks throughout the program, for good access.

Technical Sessions:

- Die Level Fault Isolation • Package Level Analysis
- System Level Analysis • Advanced Techniques
- Optical Techniques • Optoelectronic Devices
- Failure Analysis Process • Circuit Edit for FA, FI, and Debug • Case Histories • SPM Techniques
- Sample Preparation • Nanotechnology Analysis
- Yield Enhancement • Discretes, Passives, and MEMS • Metrology and Materials Analysis • Test
- plus Poster Papers

Panel Discussions:

- Strategic Development in FA. What Can We Get From Other Technical Sources?
- Can Competitors Build Some Common FA Facilities To Improve ROI And Efficiency?

Tutorials:

- Failure Analysis Basics • Device and Packaging
- Microscopy Tools • Yield • Sample Preparation
- Fault Isolation • MEMS • Failure Mechanisms
- Failure Analysis Laboratory Management

.... plus **User Group meetings** on Tuesday and Wednesday evenings, to provide a convenient forum for users of a specific technique to meet, share ideas, and discuss relevant issues in a non-commercial environment. Planned topics this year:

- Scanning Optical Microscopy (SOM)
- Scanning Probe Microscopy (SPM)
- Focused Ion Beam (FIB)
- Chip Access/Delaying
- Nano Probe

Luncheon Address:

Dr. Johannes Stork, Senior Vice President and Chief Technology Officer, Texas Instruments



As Director of the Silicon Technology Development organization, Dr. Stork's primary responsibilities are the development of advanced CMOS, packaging and mixed signal process technologies.

ISTFA is the best venue for learning new failure analysis techniques, challenges and directions. It also provides ample opportunities for you to participate and network through the question-and-answer periods, the user groups, the panel discussions, the exhibition, and the networking poster luncheon.

Additional information is on the ISTFA web site:

www.ISTFA.org

CLICK!

- Online conference registration begins Sept. 15th. Download the registration form at:
www.e-grid.net/conf/istfa-reg.pdf
- Discounted fees for EDFAS and ASM Members. Non-Members of EDFAS receive a full year's membership with their registration.

Tutorials-only and Exhibits-only registrations are available. To exhibit at ISTFA, please contact **Mr. Charles Dec**:

charles.dec@asminternational.org

EDFAS General Membership Meeting

Tuesday, November 8, 4:40-5:30 pm

The **Electronic Device Failure Analysis Society (EDFAS)** will hold its annual General Membership Meeting on Tuesday at ISTFA. It is open to all current members, as well as interested prospective members.

Antenna Systems 2005



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The premiere conference focusing on the latest advancements in Antenna Systems and Technology & Short-range Wireless Standards and Technology

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**September 22-23 – Santa Clara, CA
Santa Clara Marriott Hotel**

More than 40 technical presentations from the foremost experts on antenna systems and short-range wireless standards & technology. One registration fee provides access to both technical programs. **Antenna Systems** focuses on the most important advancements in antenna systems and technology. The co-located **Short-Range Wireless** focuses on the most recent advancements in short-range wireless standards and technology for industrial, commercial and residential applications.

Keynote Talks:

Small Size Active Controllable Antennas for Mobile Phones,
Anders Thornell-Pers, Centurion Wireless Technologies

**Subscriber Based Smart Antenna For Wireless Devices:
From Concept to System Integration And Beyond,**
Dr. Bing Chiang, Technical Staff Member, InterDigital Corp

RFID Technology: Promises and Challenges
Salil Pradhan, Chief Technology Officer, H-P RFID Prgm

Panel Discussion:

Wireless Technology Market Development & Direction

Plus three tracks of technical presentations, exhibits

General information, online conference registration, and hotel information is available on the web site:

www.antennasonline.com



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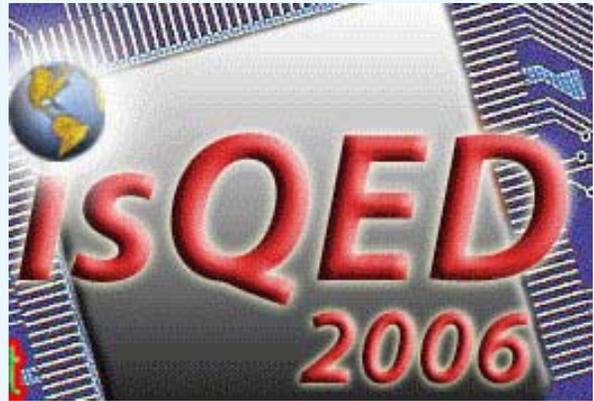
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Call for Papers

ISQED 2006 7th International Symposium on QUALITY ELECTRONIC DESIGN



March 27-29, 2006
San Jose, CA, USA

www.isqed.org



Design for Quality in the Era of Uncertainty

ISQED is the pioneer and leading international conference dealing with the design for manufacturability and quality issues front-to-back. ISQED spans three days, Monday through Wednesday, in three parallel tracks, hosting near 100 technical presentations, six keynote speakers, two-three panel discussions, workshops/tutorials and other informal meetings. Conference proceedings are published by the IEEE Computer Society and hosted in the IEL/XPLORE digital library. Proceedings CD ROMs are published by ACM. In addition, continuing the tradition of reaching a wider readership in the IC design community, ISQED will continue to publish special issues in leading journals. The authors of high quality papers will be invited to submit an extended version of their papers for the special journal issues.

Papers are requested in the following areas

- Design for Manufacturability & Quality
- Package - Design Interaction & Co-Design
- Design Verification and Design for Testability
- Embedded Test Methodologies
- Robust Device, Interconnect, and Circuits
- EDA Tools & IP Blocks; Interoperability and Implications
- Physical Design, Methodologies & Tools
- Effect of Technology on IC Design, Performance, Reliability & Yield
- Design Quality Definitions, Metrics, and Standards
- Quality Driven Design Flows; SoC, ASIC, FPGA, RF, Memory, etc.
- Quality of Modeling Abstractions and Methods (Device, Interconnect, Micro and Macro Cells, IP Blocks, ...)
- System-level Design, Methodologies & Tools
- Redundancy & Self Correction Design Techniques
- Management of Design Process, and Design Database
- Global, Social, and Economic Implications of Design Quality
- Quality based EDA Tools, Design Techniques, and Methodologies dealing with issues such as:
 - Timing Closure
 - R, L, C Extraction
 - Ground/Vdd Bounce
 - Signal Noise/Cross-Talk /Substrate Noise
 - Voltage Drop, Power Rail Integrity
 - Metal Migration, Hot Carriers
 - High Frequency Effects
 - Thermal Effects
- Power Estimation
- Plasma Induced Damage, and yield limiting effects
- EMI/EMC
- Proximity Correction & Phase Shift Methods
- Verification (Layout, Circuit, Function, etc.)
- EOS/ESD
- Packaging Modeling and Simulation

IMPORTANT DATES:

Paper Submission Deadline	October 7, 2005
Acceptance Notification	November 22-24, 2005
Final Camera-Ready Paper	January 3, 2006

Submission Process

The guidelines for the final paper format are provided on the conference web site at www.isqed.org. Authors should submit FULL-LENGTH, original, unpublished papers (Minimum 4, maximum 6 pages). To permit a blind review, do not include name(s) or affiliation(s) of the author(s) on the manuscript and abstract. Submit your papers using the on-line paper submission procedure available on the ISQED web site. Please check the as-printed appearance of your paper before submitting the paper. Address all other inquiries to publication@isqed.org.

IEEE Professional Skills Courses

Creative Problem Solving

- Date/Time: Wed Sept 14, 8:30 AM - 4:30 PM
- Instructor: Michael Burns
- Location: LSI Logic, Milpitas
- Fee: \$350 for IEEE Members; \$425 non-members

Whatever your specific goal -- your own job or business or the systems, processes or products of your company -- you can improve the quality and quantity of your new ideas. Re-energizing your right brain for creative and breakthrough thinking could be profitable personally and professionally.

Managing Time & Multiple Priorities

- Date/Time: Thursday Sept 15, 8:30 AM - 12:30 PM
- Instructor: Peter Turla
- Location: Exar Corporation, Fremont
- Fee: \$275 for IEEE Members; \$300 non-members

The way we elect to spend our time determines our success. This is a powerful course packed with time-saving ideas that you can use every day of your life.

Getting Things Done Across Organizational Borders

- Date/Time: Tuesday, Sept 20, 8:30AM-4:30PM
- Instructor: Linda Price
- Location: BEA Systems, San Jose
- Fee: \$350 for IEEE Members; \$425 non-members

"Right-sizing" and restructuring have put new emphasis on lateral communication and inter-departmental cooperation. This seminar introduces you to innovative practices for dealing with people who do not report to you-but whose assistance and support are critical. You will be provided with new perspectives on the root causes of your communication blockages with others, as well as, practical techniques for assessing the styles of others, uncovering their needs and reaching mutually satisfying agreements.

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Clear Business, Technical, and E-mail Writing

- Date/Time: Thursday, October 6, 8:30AM-4:30PM
- Instructor: Kathleen Mohn
- Location: Cypress Semiconductor, San Jose
- Fee: \$375 for IEEE Members; \$425 non-members

This workshop provides a step-by-step process for designing and writing a clear engineering document, e-mail message, or report. You will learn by doing, the only legitimate way to improve writing skills! The training involves writing, revising, and editing exercises; critiquing documents; games; and lecture. You will walk away with confidence in writing and editing skills and with a consciousness about international writing.

Leadership Skills for Engineers

- Date/Time: Wed, October 19, 8:30AM-4:30PM
- Instructor: Dr. Andrew Oravets
- Location: LSI Logic, Milpitas
- Fee: \$350 for IEEE Members; \$425 non-members

The challenges of leadership in high-tech companies have never been greater. Today's manager must be fully aware of his/her style and be able to adjust to fit the needs of others and the demands of the situation. In addition, obtaining relevant information and sharing it appropriately requires skills in phrasing questions, listening and speaking for results. This high-impact, one-day workshop provides technical managers with analytical tools and cultivates "street smarts".

Improve your skills – register for one of these classes, or for others coming up this fall. Bring a team!

For complete course information, schedule, and registration form, see our website:

www.effectivetraining.com

Consultants' Network of Silicon Valley

Consultants' Business Seminar

CBS-2005 is an educational seminar about Engineering Consulting as a career. This event has important information for both new and experienced consultants. **CBS-2005** covers the basics with topics including Rate Surveys, Best Use of Contract Broker Agencies, Contracts & Negotiations, how to use the internet to get leads, and more. Plus "Weather Reports" about What's Hot and What's Not, "What the IEEE National and IEEE AICN are up to" these days, and Current Events Issues including the realities of Off-Shoring and the opportunities for Consultants.

Saturday, October 22, 2005
8:30 AM – 4:30 PM
at Keypoint Credit Union
2805 Bowers Ave, Santa Clara

The Program is a mix of panels and speakers, with dual tracks for several one-hour sessions in morning.

**** Low Cost, High Value ****

	Early Reg'n by Oct 13, 05	Regular Reg'n after Oct 13, 05
Members	\$45.00	\$57.00
Non-Members	\$60.00	\$72.00

Includes Continental Breakfast and Sandwich-Buffer Lunch

Information: www.e-grid.net/docs/0510-scv-cnsv.pdf

TUESDAY SEPTEMBER 6

Silicon Photonics: Opportunity, Applications & Recent Results

Speaker: Mario Paniccia, Intel Corporation
Time: Networking and Pizza Social at 7:00 PM,
Presentation at 8:00 PM
Cost: none
Place: National Semiconductor Credit Union,
955 Kifer Road, Sunnyvale
RSVP: Please reserve in advance by email to
rsvp-scv-leos@ieee.org
Web: ewh.ieee.org/r6/scv/leos/

Dr. Mario Paniccia is currently the Director of Photonic Technology Lab at Intel Corporation. Mario currently directs a research group with activities in the area of Silicon Photonics. The team is focused on developing silicon-based photonic building blocks using standard CMOS processing for future use in enterprise and data center communications. Mario has worked in many areas of optical technologies during his career at Intel including optical testing for leading edge microprocessors, optical communications and optical interconnects. His teams pioneering activities in silicon photonics have led to the first silicon modulator with bandwidth >1GHz (2004) and the first continuous wave silicon laser breakthrough (2005). He has published numerous papers, including 3 Nature papers, 2 book chapters, and has over 61 patents issued or pending. Mario earned a B.S. degree in Physics in 1988 from the State University of New York at Binghamton and a Ph.D. degree in Solid State Physics from Purdue University in 1994.

Silicon photonics, especially that based upon silicon on insulator (SOI), has recently attracted a great deal of attention since it offers an opportunity for low cost opto-electronic solutions for applications ranging from telecommunications down to chip-to-chip interconnects. The presentation will give an overview of research being done at Intel in the area of Silicon Photonics. The presentation will discuss some of the practical issues and challenges with processing silicon photonic devices in a high volume CMOS manufacturing environment and present some of the recent results including the recent breakthroughs in the area of Raman amplification and CW lasing in silicon.



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WEDNESDAY SEPTEMBER 7

Introduction to the Stanford Nanofabrication Facility, with Research Examples

Speaker: Paul Rissman, PhD, Director of Research Operations, Stanford Nanofabrication Facility

Time: 7:30 PM networking, 8:00 PM presentation

Cost: none

Place: Cogswell College Room 197, 1175 Bordeaux Dr, Sunnyvale

RSVP: not required

Web: www.ewh.ieee.org/r6/scv/ims/

The Stanford Nanofabrication Facility is part of the NSF's National Nanotechnology Infrastructure Network. It is a research and development facility with a wide variety of semiconductor processing equipment that is open to external use. In a typical month, there are 200 users of the facility comprised of 120 Stanford graduate students, 20 students and faculty from other universities, and 60 industrial users, primarily from start-up companies. Projects in the lab come from the study of MEMS/NEMS, bio-MEMS/NEMS, sensors/actuators, nanotubes/nanowires, semiconductor materials and device research, magnetic technology, photonic devices and many other fields.

Paul Rissman is the Director of Research Operations of the Stanford Nanofabrication Facility at Stanford University in Palo Alto. His undergraduate and graduate education was in Electrical and Computer Engineering at the University of Wisconsin in Madison. Paul worked 26 years in the semiconductor industry, including 2 years at Amdahl Corporation, 20 years at Hewlett Packard, and 4 years at LSI Logic, serving in various management positions for the last 19 years. He has 26 publications, 4 patents granted, 2 patents filed, and 2 patents disclosed in the fields of semiconductor processing, electron beam lithography, superconducting junction technology and other fields.

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Load Pull Measurements for Device Characterization

Speaker: Steve Reyes, Focus Microwave
Time: 6:00 PM refreshments and social time, 6:30 PM presentation
Cost: none
Place: SC12-Auditorium, Intel Corp.
3600 Juliette Lane,
Santa Clara
RSVP: not required
Web: www.mtt-scv.org/sept_mtg.html

Steve Reyes is the sales and technical support manager for Focus Microwaves. He has been in the microwave test and measurement industry for more than 25 years and has held positions in product development and product marketing of microwave synthesizers, power meters, scalar and vector network analyzers. Steve has written and presented numerous papers and lectures on microwave measurements including power measurement lectures at the NIST/ARFTG Microwave Measurements Short Course. Steve is a graduate of the University of California, Davis and has an M.B.A degree from the University of Santa Clara.

Abstract:

- Intro to load-pull measurements
- Different types of tuners available - electronic and electro-mechanical
- Goals of load pull measurement systems - wideband, high VSWR, stable, harmonic tuning
- Typical system setup using a VNA - on-wafer, device test fixtures, connectorized packages
- Considerations in calibration setup - recommended calibration types, how to verify, issues related to different device types
- Principles of EM tuners - how to achieve high VSWR, how to tune for harmonics, accuracy issues, issues when measuring on-wafer
- Harmonic load pull - why it is an issue
- How to achieve harmonic load pull - frequency discriminators (Di-triplexers), harmonic rejection tuners
- Mechanical layout of EM tuner - use of probes, limitations, advantages, variations in approach and design
- Challenges in harmonic tuning - interaction between probes, vibration, system configurations
- How to achieve harmonic tuning isolation
- How to achieve zero vibration tuning
- Examples of plots - how to analyze the data for accuracy

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WEDNESDAY SEPTEMBER 14

Kirkendall Voids in Lead-Free Solder Joints: A Reliability Issue

Speaker: Zequn Mei, Cisco

Time: Seated dinner at 6:30 PM; presentation at 7:30 PM

Cost: \$25 if reserved by Sept. 11; \$30 at the door; presentation-only is free

Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale

RSVP: Please reserve and pay in advance using our PayPal on-line system or email Janis Karklins

Web: www.cpmpt.org/scv/

Zequn Mei received his Ph.D. of Materials Science and Engineering from University of California at Berkeley. He is currently working at Cisco Systems, in the Manufacturing Technology Group, on interconnect reliability.

Previous studies demonstrate extensive Kirkendall voids at the interface of a solder joint to a copper substrate, and their significant effects on the impact and shock strength of the solder joints. This talk focuses on two issues: the condition for the void formation; and the effect of voids on solder joint reliability. Samples of electronic assemblies of different packages aged or thermal-cycled were cross-sectioned by either FIB or sputtering etching. The results show that voids at the Cu/solder interface formed extensively in some cases, but not so much in others. So far, we are not clear exactly what factors control the void formation; it seems that the Cu plating process and the small concentration of Ni in either the solder or the substrate influences the void density and distribution. Shock strength at 400G of BGA packages aged for 20 days at 125°C did not degrade; the failure occurred by either delamination at the fiber/resin interface underneath the non-solder-mask-defined Cu pads, or inside the solder where they were close to the solder-mask-defined Cu pads. We also curve-fitted the result of voids growth vs time at different temperatures with the equation of $A = C t^{0.5} \exp(-Q/RT)$, to use it for prediction of the voided area at the product's service condition.

Patent Agent

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THURSDAY SEPTEMBER 15

Power System and Equipment Grounding and Personnel Protection

Speaker: Dev Paul, Earth Tech Inc.
Time: No-host social at 5:30 PM; Presentation at 6:15; Dinner at 7:15; Presentation continues at 8:00
Cost: \$22 for IEEE members;
\$25 for non-members
Place: Marie Callender's Restaurant (Garden Room); 2090 Diamond Blvd in Concord near the Concord Hilton Hotel
RSVP: by September 14, by email to Gregg Boltz at gboltz@brwncaid.com or call (925) 210-2571
Web: www.e-grid.net/docs/0509-oeb-ias.pdf

Mr. Dev Paul is a senior member of IEEE, his membership with IEEE started in 1973. He received the B.Sc. degree with honors in mathematics and the M.S.E.E. degree in electrical engineering in 1969 and 1971, respectively. He has completed further studies in power systems at the University of Santa Clara.

He joined Kaiser Engineers, Oakland, CA. in 1972 as a design engineer and now the same company is EARTH TECH Inc, part of TYCO International. Mr. Paul has worked on a variety of heavy industrial, co-generation, commercial, DOD and DOE facilities, and rapid transit rail projects. In his present position as a Chief Electrical and Project Manager, he is responsible for the overall design, analysis, studies, specifications, installation, project management, system startup and system integration work on variety of projects. He has authored twelve (12) technical papers, which are published in IEEE Industry Applications Society (IAS) Transactions and American Public Transit Association (APTA) conference proceedings. His main fields of interests are power system analysis, protection, grounding and harmonics.

Mr. Paul is an active member of several IAS Committees. He has served as a treasurer and vice chairman for the local IEEE Chapter. He is a registered Professional Engineer in the States of California, Nevada, and Oregon. He received the IEEE Ralph H Lee Award for his Technical Paper on DC Power System Grounding in 2003. He is presently a Chairman of the Power System Surge Protection Standard.

The September IAS meeting features a technical presentation by Mr. Dev Paul on the subject of "Power System and Equipment Grounding and Personnel Protection." He will also cover issues related to grounding and the bonding of down conductors involved in the design of a Lightning Protection scheme.

Recently Mr. Paul presented technical papers at IEEE/IAS conferences on the two different subjects: 1) Lightning Protection and 2) Shore-to-Ship Power Supplies(Cold Ironing)-Power System Grounding and Safety Analysis. The technical highlights from both of these papers, as related to personnel and equipment protection, will be combined and covered in this presentation.

The speaker will add further interest in the discussion of personnel protection by providing examples of actual designs taken from industrial, commercial, rapid transit systems and Port facilities. Contradicting and conflicting design issues will also be addressed. Lastly, for a better understanding of personnel protection, the equivalent electrical circuit of the human body will be reviewed and discussed from a present day and historical viewpoint. There will be ample time for questions and answers during and after the presentation.



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TUESDAY SEPTEMBER 20

Silicon Valley: The BioTransformation of the Valley and Opportunities for Engineers

Speaker: Dr. Sudhi Gautam, Founder & Medical Director, Med Tech Bridge
Time: 7:00 PM Networking, 7:30 PM Presentation
Cost: none
Place: Keypoint Credit Union, 2805 Bowers Ave, Santa Clara (map)
RSVP: not required
Web: www.ieee-sv-consult.org/notices.htm

This talk will focus on the Biotransformation that is underway in the Silicon Valley, to give an overview of the Local Biomedical industry and identify opportunities for engineers in the newly emerging Biomedical Wave. This talk is geared towards engineers who want to catch the Biomedical Wave and transition their current strengths/skills into the Medical Device, Healthcare, Biomedical, Clinical Trials or Biotech industries.

Dr. Sudhi Gautam is a versatile, high-energy Surgeon-Scientist-Technologist who has over 15 years of cross-disciplinary expertise in Surgery, Artificial Biohybrid Organs, Medical Devices, Internet Technology, Medical Informatics, Medical Education and Engineering Technology. He currently holds the position of Executive-in-residence at Girvan Institute, a technology incubator in Santa Clara. Prior to this, he was at the Medical division of Sanmina-SCI, a global Electronics Manufacturer. Dr. Gautam completed post-doctoral research at the Univ of Michigan, Ann Arbor, and practiced ENT surgery for over 6 years before completing his Ph.D. in Biomed Engineering at the IIT, Bombay.

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Information: www.e-grid.net/docs/0510-scv-cnsv.pdf

SCV Magnetics

TUESDAY SEPTEMBER 20

Recording Performance of Discrete Track Media

Speaker: Wen Jiang, Komag
Time: Coffee and conversation at 7:30 PM;
Presentation at 8:00 PM
Cost: none
Place: Komag, 1710 Automation Parkway, San Jose
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/mag/

For additional details, see the SCV Magnetics Society Chapter website.

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SF Communications

TUESDAY SEPTEMBER 20

Technology and Policy Roundtable: SBC Addresses IPTV, Fiber, Triple Play

Speaker: Ralph Ballart, V.P., SBC Laboratories, Inc.
Time: Presentation at 6:30 PM
Cost: none
Place: California Public Utilities Commission,
505 Van Ness Ave, San Francisco
RSVP: Please reserve by email at
sfComSoc@ieee.org
Web: ieee.org/sfcomsoc/

For additional details, see the SF Communications Society Chapter website.

Ralph Ballart is VP, Broadband Infrastructure and Services, at SBC Laboratories, Inc. Ralph's organization is responsible for broadband network element requirements and approval for use testing for SBC. Ralph began his career with Bell Labs in 1980 and worked on SONET and other transport and switching projects while with Bellcore. Ralph has a PhD in Physics from the University of Arizona.



WEDNESDAY SEPTEMBER 21

Computer-aided Detection in Diagnostic Imaging

Speaker: Sandra Stapleton
Time: 6:15 PM: dinner with the speaker in the Stanford Hospital cafeteria; presentation at 7:30 PM in Clark Auditorium at the Stanford hospital
Cost: none
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/embs/

Sandra Stapleton is currently working as a consultant developing technology and business development strategies for emerging CAD companies. Previously she was Vice President of Technology at R2 Technology, Inc., the company which developed and commercialized the first CAD systems for mammography and thoracic computed tomography (CT). More recently, she was Senior Vice President of Business Development for Medicsight, an emerging CAD company which obtained the first FDA clearance for a colon CAD product. Ms Stapleton has a Masters Degree in Medical Biophysics from the University of Toronto, Canada, where her graduate work focused on using computational analysis to quantify brain deficits due to stroke and dementia as seen on single photon emission computed tomography (SPECT) scans.

Computer-aided detection (CAD) techniques have been under investigation for nearly two decades, with most initial work aimed at helping radiologists detect breast cancer with mammography. This pioneering work focusing on CAD as a "detection" aid for mammography has led to the commercialization of several mammography CAD systems and the adoption of CAD by a large number of hospitals and breast centers -- over 2000 mammography CAD systems are in clinical use today. More recently, CAD systems have been developed for other clinical applications, including colon and thoracic analysis packages. With the development of these and other new CAD applications, CAD is evolving from a "detection" aid that provides a second opinion, to a tool integral to the clinical review process.

Using mammography CAD as a case study, Ms Stapleton will present an overview of CAD technology and the path to commercializing a CAD application, followed by a discussion of new CAD applications and their application to improving the decision making process across the clinical enterprise.

WEDNESDAY SEPTEMBER 21

An Overview of MOSFET Device Behavior and Modeling for Mixed-signal/RF IC Design

Speaker: Yuhua Cheng, Siliconlinx, Inc.
Time: 6:00 PM - Pizza, 6:15 PM - Presentation
Place: National Semiconductor Building 31 Auditorium, 955 Kifer Road, Sunnyvale
Cost: none
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/

Yuhua Cheng received the B.S. degree in electrical engineering, Shandong Polytechnic University (now Shandong University), Jinan, China in 1982, the M. S. degree in electrical engineering, Tianjin University, Tianjin, China in 1985, and the Ph.D. degree in electrical engineering, Tsinghua University, Beijing, China in 1989. In 1990, he joined in the Institute of Microelectronics as a research fellow in the Department of Computer Science and Technology (DCST), Peking University, China. From 1992 to 1996, he was an associate professor in DCST. From 1994 to 1995, he was a Visiting Professor at the Norwegian University of Science and Technology, Trondheim, Norway, and a Research Fellow of the Norwegian National Research Council. From 1995 to 1997, he was a Senior Scientist at the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley. In 1997, he worked first for Cadence Design Systems as a Member of the Consultant Staff and then joined Rockwell International. From 1997-2004, he worked for Rockwell Semiconductor Systems, Conexant Systems (a spin-off from Rockwell), and Skyworks Solutions (a spin-off from Conexant), where he was principal engineer, manager, and senior manager of mixed-signal/RF device (bipolar, MOS and passive) and technology team responsible for Mixed-signal/RF device technology development, modeling and technology support for various (ASIC, analog, Mixed-signal, RF) circuit designs. He is currently with Siliconlinx, Inc., which offers products and services to bridge the gap between IC designers and manufacturing foundries.

This talk reviews the device behavior and modeling challenges in RF CMOS technology, which is an attractive process candidate for wireless communication and system-on-chip (SOC) applications. The downscaling trend of CMOS technology will be discussed briefly. Then the MOS device characteristics will be reviewed to understand the device behavior at high frequency. Modeling issues will be explored with a focus on MOSFET devices with a discussion on device figures of merits and model validations to generate high quality models for mixed-signal/RF applications.

Biography (continued)

He has served on many technical program committees and chaired international conferences, including the IEEE Custom Integrated Circuits Conference (CICC) since 2001 and Radio Frequency Integrated Circuits Symposium since 2002. He organized and participated in several workshops and panels related to RFCMOS technology and SOC design. He has authored and co-authored over 80 research papers, several book chapters, two books "MOSFET Modeling & BSIM3 User's Guide" by Kluwer Academic Publishers, and "Device modeling for analog/RF circuit design" by John Wiley and Sons.

He is a senior member of IEEE and an EDS Distinguished Lecturer. He serves the Administration Committee of IEEE Electron Device Society (EDS). He is a member of the Membership Committee and a member of the Regions/Chapter Committee of IEEE EDS and the vice-chair of the North America West subcommittee for Regions/Chapters (SRC-NAW) of the EDS Regions/Chapters Committee.

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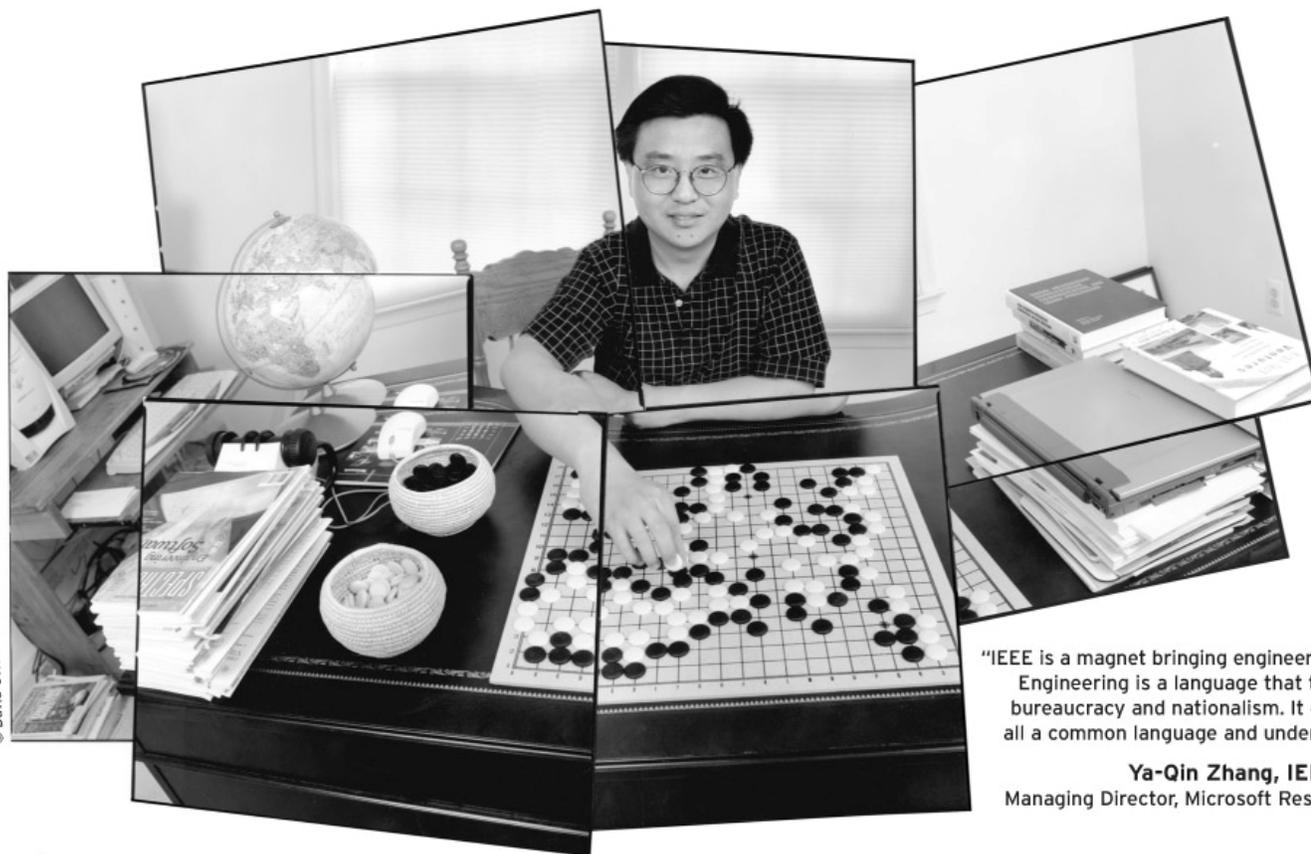
Happy Hour With Billiards @ Jillian's

Event: An evening of billiards, appetizers and drinks with fellow IEEE GOLD members
Time: 6:30 PM til ???
Place: Jillian's Billiards, 101 4th Street (near Powell Street BART Station), San Francisco
Cost: no-host; billiards/snacks provided
RSVP: not required
Web: www.e-grid.net/docs/0509-goldsf.pdf

IEEE GOLD Members, Non Members, and all interested parties and their guests are invited -- the San Francisco Chapter of IEEE GOLD would like to invite you to an evening of billiards, appetizers and drinks with fellow IEEE GOLD members at Jillian's Billiards, in downtown San Francisco (located just around the corner from the Powell Street BART Station). Billiard tables and snacks will be courtesy of S.F. GOLD.

IEEE Graduates Of the Last Decade (GOLD) is an affinity group sponsored by the San Francisco IEEE Section covering the City and the North Bay region. The group exists to help new engineers bridge the transition from a student into a career professional and to develop strong networking ties in the area's engineering community – plus to foster personal and professional growth.

Please join us for what we expect to be a great evening.



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Ya-Qin Zhang, IEEE Fellow
Managing Director, Microsoft Research Asia



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THURSDAY SEPTEMBER 22

Robert Noyce: The Man Behind the Microchip

Speaker: Dr. Leslie Berlin, Visiting Scholar & Author, Stanford University

Time: buffet lunch at 11:45 AM; presentation at 12:15 PM

Cost: \$15 if reserved by Sept. 18; \$20 at the door

Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale

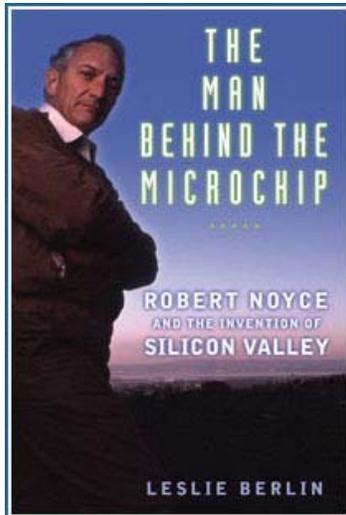
RSVP: Please reserve and pay in advance using our PayPal on-line system or email John Jackson at john.jackson@analog.com

Web: www.cpmt.org/scv/

Dr. Leslie Berlin is a Visiting Scholar in the History and Philosophy of Science and Technology at Stanford, Berlin is also Project Historian for the Silicon Valley Archives, a division of the Stanford University Department of Special Collections. In this capacity, she is working to find and preserve key papers and artifacts pertaining to the history of Silicon Valley. A former speechwriter for a Fortune 500 CEO, Berlin holds a Ph.D. in History from Stanford and a B.A. in American Studies from Yale. She lives in the San Francisco Bay Area. She is a consultant to the Intel Museum retrospective on Noyce's life which opened on June 13, 2005.



To find out more about Dr. Berlin's book on Robert Noyce, please click on the book cover.



Hailed as the Thomas Edison and Henry Ford of Silicon Valley, Robert Noyce co-founded Fairchild Semiconductor and Intel and also co-invented the integrated circuit. He was a brilliant inventor, a leading entrepreneur, and a daring risk-taker who piloted his own jets and skied mountains accessible only by helicopter. Leslie Berlin spent nearly a decade studying Noyce's life, and her recently published biography, **The Man Behind the Microchip: Robert Noyce and the Invention of Silicon Valley**, has received praised from engineers, businesspeople, and academics alike. In this talk based on her research, Berlin captures not only Noyce's work but also the vibrant interplay of technology, business, money, politics, and culture that defines Silicon Valley.

Leslie will give us insight into Robert Noyce the person and the entrepreneur, and what she found out as she researched his life. Noyce came to the Bay Area to work for the brilliant Nobel-prizewinning physicist William Shockley. In September 1957, Noyce and seven other Shockley employees, frustrated by the challenges of working for the mercurial Shockley, decamped to start their own firm to build silicon-based transistors. This move, which launched Fairchild Semiconductor, is often cited as the first in the chain of events that launched Silicon Valley. In 1968, Noyce and Gordon Moore, another member of the group of eight that started Fairchild Semiconductor, decided to launch another startup company. Today that firm is called Intel, the largest semiconductor company in the world. Noyce led Intel for seven years as president and another fifteen as a director.

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TUESDAY SEPTEMBER 27

Overview of IEEE Standard 1015-1997 ("Blue Book")-- "Recommended Practice for Applying Low-Voltage Circuit Breakers Used in Industrial and Commercial Power Systems"

Speaker: David D. Roybal, Eaton Corporation

Time: Social at 5:30 PM, Presentation at 6:00 PM,
Dinner at 7:00 PM

Cost: \$25 (at the door)

Place: Sinbad's Restaurant, Pier 2 The
Embarcadero, San Francisco
(415.781.2555)

RSVP: Please preregister by email at
jlin@sfwater.org to qualify for the drawing

Web: www.ewh.ieee.org/r6/san_francisco/ias

David D. Roybal received the Bachelor of Science degree in electrical engineering from Santa Clara University in 1969. He is a Fellow Application Engineer with Eaton Corporation in Livermore. He previously was an engineer with Westinghouse for more than 24 years. Mr. Roybal is a Senior Member of the IEEE who has served as an officer of the San Francisco chapter of the IEEE-IAS, the IEEE San Francisco Section, and the IEEE Bay Area Council. He is a member of NFPA, NSPE, and chairman of the NEMA California Safety Regulations Advisory Committee. He is chapter secretary for the International Association of Electrical Inspectors (IAEI), a member of the Executive Board of the California Electrical Inspectors (CEI), and a registered professional engineer. He has had three papers published by IEEE on the subject of circuit breakers.

This presentation will be an overview of the IEEE Blue Book which provides information for selecting the proper circuit breaker for a particular application. This information helps an engineer specify the type of circuit breaker, ratings, trip functions, accessories, acceptance tests, and maintenance requirements required. It will include a discussion of circuit breakers for special applications, application at different points in the power system, and selective coordination, as well as a comparison between the standards of low-voltage power circuit breakers and molded-case circuit breakers.

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Built-In Soft Error Resilience for Robust System Design

Speaker: Subhasish Mitra, Intel Corporation
Time: 6:30 PM - refreshments;
7:00 PM - presentation
Cost: none
Place: H-P Oak Room, Bldg 48, Cupertino, just North of Fwy 280 (Wolfe Rd Exit) at the corner of Pruneridge Ave. and Wolfe Rd.
RSVP: not required
Web: ewh.ieee.org/r6/scv/rs/

Dr. Subhasish Mitra is a Principal Engineer at Intel Corporation where he is responsible for developing enabling technologies for robust system design -- Design for Reliability, Testability and Debug -- in advanced technologies. He is also a Consulting Assistant Professor in the Electrical Engineering Department of Stanford University, and the Associate Director of the Stanford Center for Reliable Computing. Before joining Intel, he led the Stanford project on "Reliability Obtained by Adaptive Reconfiguration" sponsored by DARPA as part of the Adaptive Computing Systems program. He also consulted for several companies including Agilent Technologies Laboratories. His research interests include robust system design, VLSI design and test, CAD, fault-tolerant computing and computer architecture. He received Ph.D. in Electrical Engineering from Stanford University.

Dr. Mitra has published more than 70 technical papers in leading conferences and journals, and invented design and test techniques that have seen wide-spread proliferation in the industry. He has received several awards, including the 2005 IEEE Circuits and Systems Society Donald O. Pederson Award for the Best Paper published in the IEEE Transactions on CAD, and the 2004 Intel Achievement Award, Intel's highest corporate award, "for the development and deployment of a breakthrough test compression technology."

Radiation-induced logic soft errors in flip-flops and combinational logic pose a major challenge in the design of robust systems for enterprise computing and networking applications. In the past, soft errors were of concern especially for space applications. Increasing system-level soft error rates in advanced technologies, and stringent system data integrity requirements demand special design techniques to protect systems from logic soft errors. This talk will discuss the impact of technology scaling on soft error rates, evaluation of run-time behaviors of systems in the presence of soft errors, and design of robust architectures incorporating Built-in-Soft-Error-Resilience (BISER) techniques. Design-for-test and debug resources are reused for soft error protection during normal system operation, resulting in 20-fold reduction in flip-flop soft error rate, with negligible area and speed impact, and 3-5% system-level power overhead. In comparison, classical redundancy techniques introduce 40-100% power, performance and area overheads.

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TUESDAY OCTOBER 4

Annual Banquet: The Future of California Energy

Keynote Speaker: Yakout Mansour, CEO, CA-ISO
Time: Social at 5:00 PM, Dinner at 6:00 PM, Presentation at 7:00 PM
Cost: \$30 Early Bird Special before September 23rd, \$35 afterward; , Students - \$15, group/table rates available
Place: Sinbad's Restaurant, 2 Embarcadero (Pier 2), SF -- free validated parking on Pier 2
RSVP: Please fill out and return the Reservation and Dinner Choice form
Web: www.e-grid.net/docs/0510-sf-pes.pdf

Recent actions by Congress and other developments in FERC policies have raised questions about the future of the California energy industry. The recently passed Energy Bill and the 2003 NE Blackout have triggered the need to re-examine and mandate NERC reliability standards and evaluate the adequacy and security of system infrastructure. How will these issues affect the California Independent System Operator (CA-ISO), and how is their reorganization positioning them for the future?

Yakout Mansour, CEO of the CA-ISO, will discuss these issues in detail as the keynote speaker for this event. SF PES will host a short annual awards ceremony during this event. Awards will be presented to notable contributors to the IEEE and the Power Engineering Society. In addition, attendees will enjoy fine dining at Sinbad's Restaurant. Dinner is subsidized by the SF PES ADCOM committee, so that all attendees can enjoy this great memorable evening at a reasonable price. This will be an enjoyable evening for engineers and non-engineers alike, so invite a friend or family member. All are welcome!

SF PES is offering a group discount to this event. Purchase a table for 10 attendees at a price of \$250. Corporate Sponsorships are available for \$100. Call for details.

Please make your dinner selections using the form at this location:

www.e-grid.net/docs/0510-sf-pes.pdf

WEDNESDAY OCTOBER 12

Imprint Patterning: An Alternative Circuit Fabrication Process

Speaker: Dr. Craig Davidson, Dimensional Circuits
Time: Seated dinner at 6:30 PM;
presentation at 7:30 PM
Cost: \$25 if reserved by Oct. 9; \$30 at the door;
presentation-only is free
Place: Ramada Inn, 1217 Wildwood Ave (Fwy
101 frontage road, between Lawrence
Expy and Great America Pkwy),
Sunnyvale
RSVP: Please reserve and pay in advance using
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A new approach to fabricating printed circuits named Imprint Patterning™ will be described. In conventional printed circuit fabrication two major process elements -- photolithography and laser drilling -- contribute significantly to performance constraints and cost. Imprint Patterning replaces these two steps with a single cost-effective microreplication operation that results in huge cost and performance advantages. These same techniques are used today to fabricate CDs and DVDs with high quality and low cost. And they are on the semiconductor technology roadmap for the sub-40 nm nodes. Dimensional Imprint Technology, Inc. is commercializing Imprint Patterning for the printed circuit industry.

Dr. Craig Davidson is Sr. VP and Chief Technology Officer of Dimensional Imprint Technology, Inc. He has expertise in various high technology industries including electronics and aerospace. Dr. Davidson was previously the VP of Technology for Multilayer Technology, Inc. (Multek) the 12th largest PCB supplier in the world and a wholly owned subsidiary of Flextronics International. His career spans printed circuit fabrication, semiconductor packaging, and card-level assembly processes. Dr. Davidson's degrees are in Chemistry and Materials Science. He holds 7 patents and is widely published in the technical literature.

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THURSDAY OCTOBER 13

AC Control Power and Digital Protective Relays: Avoiding the Pitfalls

Speaker: Gary Fox, GE Industrial
Time: No-host social at 5:30 PM; Presentation at 6:15; Dinner at 7:15; Presentation continues at 8:00
Cost: \$22 for IEEE members; \$25 for non-members
Place: Marie Callender's Restaurant (Garden Room); 2090 Diamond Blvd in Concord near the Concord Hilton Hotel
RSVP: by October 12, by email to Gregg Boltz at gboltz@brwncald.com or call (925) 210-2571
Web: www.e-grid.net/docs/0510-oeb-ias.pdf

Gary H. Fox received his BSEE from California Polytechnic State University, San Luis Obispo in 1978. He became a Member of IEEE in 1989, and a Senior Member in 2001. He has been employed by General Electric Company for 27 years. His current assignment is a Systems Engineer for GE Industrial in Concord, providing application and technical support for power distribution and control equipment. Mr. Fox is a member of the IEEE Industry Applications and IEEE Power Engineering Societies. He has held several IEEE officer positions including Chair for the San Francisco Chapter, IAS; Chair, San Francisco Section; and Chair, San Francisco Bay Area Council. In addition, he has lectured at several local IEEE workshops covering the subjects of high voltage substation design, short circuit calculations, and power system protection. He has been a Professional Engineer licensed in California since 1982.

The October IAS meeting features a talk entitled "AC Control Power and Digital Protective Relays: Avoiding the Pitfalls." The speaker will be Gary H. Fox, P.E., Systems Engineer with GE Industrial.

Batteries are considered to be the most reliable control power source used in medium voltage switchgear. But applying batteries can cause headaches for the design professional, or owners simply don't like the amount of space they use up. So ac control power is often used as an alternative. This would be fine if we were still using electromechanical relays for protection. But digital relays have become the default choice for protection on modern switchgear and most digital relays require a separate control power source for their operation. If that control power is an ac source derived from the primary circuits, the voltage to the protective relays cannot be considered to be reliable and compromises the protection of the circuit. At this chapter meeting, an IEEE paper originally presented at the 2005 IAS Pulp and Paper Industry Conference will be discussed that explores the issues surrounding ac control power, and techniques that can be applied to mitigate those issues.



THURSDAY OCTOBER 27

Drop-Testing of Components in Portable Applications

Speaker: Dr. Luu Nguyen, National Semiconductor
Time: buffet lunch at 11:45 AM;
presentation at 12:15 PM
Cost: \$15 if reserved by Oct. 23; \$20 at the door
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Please reserve and pay in advance using our PayPal on-line system or email John Jackson at john.jackson@analog.com
Web: www.cpmt.org/scv/

Dr. L. T. Nguyen is a Senior Engineering Manager in the Package Technology Group at National Semiconductor Corp, working on various aspects of wafer-level packaging, lead-free and halogen-free, thermal measurement and modeling, and design-for-manufacturability. He co-edited two books on packaging, and has over 190 publications. He has over 50 patents and invention disclosures. He is a Fellow of IEEE and ASME, and a Fulbright Scholar (Finland 2002). He is currently an Associate Editor for the CPMT Transactions on Advanced Packaging and a Guest Editor for the CPMT Transactions on Components and Packaging Technologies. He received two Best of Conference Awards (27th IEMT 2002 and InterPack 2005) and eight IMAPS and IEMT Best of Session Conference Awards. Other awards include the 2003 Mahboob Khan Outstanding Mentor Award from the Semiconductor Research Corporation in recognition of contributions to student mentoring, research collaboration, and technology transfer, and the 2004 IEEE CPMT Society's Outstanding Sustained Technical Contributions Award.

Portable devices such as cell phones and PDAs are more likely to be dropped than affected by changes in thermal conditions. As a result, current reliability research has shifted from studying the effects of typical thermomechanical cycling to mechanical shock. Technical challenges arise from the complexity of lead-free solder metallurgies, printed wiring board finishes, and component metalizations.

Earlier studies have shown that intermetallic layers between lead-free solders and component metalizations are prone to fail in drop tests. Reactions between Ni(P)/Au coated pads on PWBs and solder alloys have been studied extensively. However, much less is known about the effects of component UBM (Under Bump Metalization) with different finishes and pad structures on lead-free and tin-lead assemblies under shock loading.

This talk will discuss the behavior of two UBMs used in wafer level chip scale packages on drop test performance, namely, (Al)Ni(V)/Cu metalization and electroless Ni(P)/Au metalization. A significant difference in the reliability performance of the components was observed: those with (Al)Ni(V)/Cu UBM were more reliable than those with electroless Ni(P)/Au UBM, regardless of the solder bump type, the solder paste, the surface finish of the boards, or the pad structure on the boards. The primary failure mode in the component side is the cracking of the interconnections along a brittle NiSnP layer between the electroless Ni(P) of high P-content and the solder alloy. Components with (Al)Ni(V)/Cu, on the other hand, fail by cracking along the [Cu,Ni]6Sn5 layer. On the board side, cracking happens in the porous NiSnP layer formed between the electroless Ni(P) metalization and the [Cu,Ni]6Sn5 intermetallic layer. Cracking happens predominantly on the component side due to three factors:

- high stresses on the component side;
- brittleness of the reaction layers; and,
- strain-rate hardening of the solder interconnections.

It will be shown that such failure mode differs from that typically observed in thermally cycled devices, where the nucleation and propagation of cracks are strongly enhanced by the recrystallization of the solder interconnects.

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CONFERENCE CALENDAR

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www.e-grid.net/docs/conf-flyer.pdf

September 13-15: International Symposium on Semiconductor Manufacturing

- San Jose Fairmont Hotel
- Workshops: Monday, September 12
- Sessions: Tuesday – Thursday

The 14th ISSM will be held at the San Jose Fairmont Hotel. ISSM is the largest world-wide forum specifically designed for semiconductor device manufacturers and suppliers.

See **Page 4** for more details

Sept 22-23: Antenna Systems and Short-Range Wireless Conferences

Held this year at the Santa Clara Marriott, these co-located events bring together the foremost experts on antenna systems and short-range wireless standards & technology.

Early-bird discount through August 19th

See **Page 5** for more details

Oct 24-27: GSPx: Pervasive Signal Processing Conference and Expo

- Santa Clara Convention Center
- Workshops: Monday, October 24
- Sessions & Expo: Tuesday – Thursday

This major event focuses on embedded signal processing and the myriad of applications that the technology is spawning.

Note that there are substantial GRID & Early-bird discounts through September 15th.

See www.e-grid.net/conf/gspix.html
for more details

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