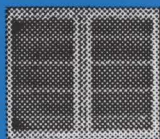


IEEE

Solid-State Circuits



Newsletter

Volume 1 Number 3

August 1996

Message From The President

Robert G. Swartz rgswartz@ix.netcom.com
President IEEE Solid-State Circuits Council

The last few months have been a tumultuous time for the IC design community, and for me personally. We have witnessed feverish activity in some areas of our industry, softening of demand in others, and confusing gyrations in the semiconductor Book-to-Bill ratio. Yet the health of our profession is strong, and attendance at IEEE-sponsored IC design conferences approaches record levels. Seeking new personal challenges, I myself departed AT&T Bell Laboratories, my employer of 17 years, and moved from New Jersey to Silicon Valley. There, in moments of transcendental insight, I discovered that the automobile traffic is amazingly bad, the weather is terrifically good, and the cost of housing exceeds the limits of mortal comprehension. None of this is news to you, of course. But Silicon Valley is also the heart of our industry, and it is at once apparent to any who visit here that the heart beats strongly. Where else do you find highway billboards advertising standard cell libraries, local radio news programs sponsored by IC CAD companies, or the visible enthusiasm of every commuter to get to work???

Plans for the new Solid-State Circuits Society continue apace. This June, the IEEE Board of Directors gave their final approval for the Society. It's a done deal, effective January 1, 1997.

Meanwhile, we have several items on the agenda for you. The two most important are elections and membership enrollment.

The Solid-State Circuits Society will hold its first elections this fall. In the previous issue of the Newsletter, we told you about the plan to select the first 5 elected members of the Society's Administrative Committee (AdCom), and we called

for nominations. Elsewhere in this Newsletter, you will find an update by David Pricer on the upcoming elections. Note that petition candidates are welcome. Please take an interest - vote!

Also this autumn, you will receive your annual IEEE membership renewal form. *If you are now a subscriber to the Journal of Solid-State Circuits, your IEEE renewal form will automatically list you as a new member of the Solid-State Circuits Society, and you do not have to do anything additional to become a member when you renew.* The membership will not cost you anything extra. Your cost for membership, including the Journal, will be exactly the same - \$14, as you are now paying for the Journal.

Lastly, the Solid-State Circuits Society is preparing to enter the modern age of electronic distribution of Society publications. In particular, we are planning to provide new and back issues of the Journal of Solid-State Circuits and other publications on CD-ROM. We are also considering an initiative to offer some publication material via the WWW. What is your opinion on this? What do you like (or dislike) about these ideas? Do you have other suggestions? Please get back to me (rgswartz@ix.netcom.com) with any thoughts on the matter.

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The Institute of Electrical and Electronics Engineers, Inc

First General Election To Be Held this Fall

Dave Pricer

dpricer@vnet.ibm.com

In a few weeks each of you will have the opportunity to participate in the first general election to determine who will govern our new Society. For the purposes of this first election, subscribers to the IEEE Journal of Solid-State Circuits will be the electorate! Five new members to the Administrative Committee will be elected this Fall.

Your interest and participation is important. The people you elect will be setting the direction of our new Society for years to come. The Nominating Committee has striven to give you a choice between candidates of varying background and interest, but who share a common interest and commitment to Solid-State Circuits. If you have regularly read the issues of the 'Journal', participated in the evening discussion sessions of ISSCC, or attended CICC, or the VLSI Symposium. You will probably recognize many of the following candidates:

NICKY LU

Nicky Lu received the B.S.E.E. degree from National Taiwan University in 1975 and the M.S. and Ph.D. degrees from Stanford University in 1978 and 1981, respectively. He is President and Chairman of Etron Technology Inc, which he founded in Taiwan in 1991. Etron is the largest fabless memory-specialty company in Taiwan, (\$55M revenue), shipping SRAM and DRAM products world wide. Dr. Lu is one of the key technical architects of the Taiwan National Submicron Project with the Taiwan Industrial Technology Research Institute to develop 8" wafer DRAM technology. Etron created the first 16M DRAM and 4M SRAM in Taiwan. The success of this project brought the Taiwan semiconductor industry to international prominence. He also started several other companies including DiC Co. in Silicon Valley, which specializes in RF design for wireless communications.

Before founding Etron, he worked at the IBM Research Center and the headquarters of the IBM Technology Products Group. He pioneered the concept of High-Speed DRAM (HSDRAM) and led the design of the world's fastest DRAM. He is co-inventor of the the substrate-plate trench capacitor (SPT) cell concept, used in IBM's 4M and 256M DRAMs. He served on the Technical Staff of the IBM Director of Research and as a Program Manager at the Technical Products Group Headquarters. He received several IBM Outstanding Innovation Awards and Outstanding Technical Achievement Awards, an

IBM Corporate Award, and the Seventh Invention Achievement Award.

He is on the ISSCC and Symposium on VLSI Circuits Program Committees, has published over 50 technical papers and has over 20 US patents. He was elected IEEE Fellow in 1990 for contribution to semiconductor memory design and technology.

CHRIS MANGELSDORF

Chris Mangelsdorf received the B.S. in physics, magna cum laude, from Davidson College, Davidson, NC in 1977. In 1980 and 1984 he received M.S. and Ph.D degrees in Electrical Engineering at MIT, where he held the Analog Devices Fellowship.

He has been associated with Analog Devices since summer employment in 1980; and is presently Senior Staff Scientist. One of his ADC products received a vendor award from Hewlett Packard and was voted one of the EDN Magazine's "Best Products of 1988." Chris is currently the Director of the Japan Design Center for Analog Devices in Tokyo.

His past research work includes cryogenics, high-voltage dielectrics and numerical simulation of electric field problems. His current interest is in analog integrated circuits, including high-speed analog-to-digital converter architectures, sample-and-holds, low-noise signal CMOS signal processing, imaging circuitry and dynamic test techniques.

He is a member of Phi Beta Kapa and Sigma Pi Sigma (physics). He has served on the Program Committee for ISSCC for five years and the Bipolar Circuits and Technology Meeting for four years. He has organized and moderated three ISSCC panels in the last five years; and received the 1993 Best Panel Award for "The Future Role of the Analog Designer."

TOSHIKI MASUHARA

Toshiaki Masuhara was born on March 5th 1945 in Toyonaka City, Osaka, Japan. He obtained the B.S. and M.S. degrees in Electrical Engineering from the University of Kyoto in 1967 and 1969. He obtained the Ph.D degree in Electrical Engineering from the University of Kyoto in 1977.

From 1969 to 1974, he was a member of the technical staff in the 3rd and 7th Departments at Hitachi Central Research Laboratory, Kokubunji, Tokyo, Japan, where he initially worked on depletion-load nMOS integrated circuits and later on modeling and analysis of MOS transistors. From 1974 to 1975 he was a special student in the Electrical Engineering and Computer Science

... continued on page 4

Membership Invitation

You will soon receive your 1997 IEEE Membership Invoice for renewing your IEEE membership for 1997. With this renewal you have a unique opportunity to become a charter member of the new Solid-State Circuits Society. If you are a subscriber of the Journal of Solid-State Circuits, your membership is free and you automatically become a member of the new Society. Your membership will be listed in section 2 on the membership invoice as shown below. If you are not a subscriber, you can join the new Society and receive your own copy of the Journal for the normal

subscription fee of \$14. In this case, you will need to add the new society membership and publication designation in section 3 of the membership invoice form.

The Solid-State Circuits Council appreciates your past support and looks forward to your continued support within the new Solid-State Circuits Society.

Please address questions to:

Charles (Chuck) W. Gwyn

gwyncw@smtplink.mdl.sandia.gov

Membership Chairman - Solid-State Circuits Society

| 1997 IEEE Membership Invoice | | | | | | |
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Journal subscription

and Computer Science Department of the University of California, Berkeley. There he worked on double-diffused MOS transistors and a new CMOS process. In 1975 he returned to Hitachi Central Research Laboratory and initiated a project to develop new high-speed CMOS static memories with nMOS cells.

In 1987 he became department manager of the 7th Department, ULSI Research Center of Hitachi Central Research Laboratory and was responsible for the design of VLSIs. He became the department manager of the 1st Department in 1990 where he supervised research groups working in high speed GaAs and bipolar integrated circuits, solar cells, imager tubes, quantum devices and research on materials. From 1991 to 1993 he was in the Telecommunications Division of Hitachi where he was responsible for the design of VLSIs components and printed circuit boards. In 1993, he assumed his current position, General Manager, Technology Development Operations, Semiconductor & IC Division, Hitachi Ltd., where he is responsible for development of process, packaging and CAD/CD for LSI.

He is a member of the Institute of Electrical Information and Communication Engineers of Japan. He was the Program Co-Chairman and the Program Chairman of the 1992 and 1993 Symposium on VLSI Circuits. He is presently the Co-Chairman and Chairman of the 1996 and 1997 Symposium on VLSI Circuits.

He received the 1990 IEEE Solid State Circuits Award for contributions to nMOS depletion-load circuits and development of high-speed CMOS memories. In 1994 he was elected IEEE Fellow "For contribution in the invention and development of nMOS circuits and high-speed CMOS static memories." He received: The Significant Invention Award, Japan 1994; Significant Invention Awards Tokyo, Japan 1994, 1995, 1988, 1992; Significant Invention Awards, Yamanashi, Japan in 1995.

BEHZAD RAZAVI

Behzad Razavi received the B.Sc. degree in Electrical Engineering from Tehran (Sharif) University of Technology, Tehran, Iran in 1985; and the M.Sc and Ph.D degrees in Electrical Engineering from Stanford University, Stanford, CA, in 1988 and 1991, respectively.

From December 1991 to January 1996 he was a Member of

Technical Staff at AT&T Bell Laboratories, Holmdel, NJ, where his research involved integrated circuit design for communications and RF systems. In January, 1996, he joined Hewlett-Packard Laboratories, Palo Alto, CA. His current interests include wireless transceivers, phase-locking and clock recovery, data conversion and frequency synthesis.

He has been a Visiting Lecturer at Princeton University, Princeton, NJ, and Stanford University. He is a member of the ISSCC Program Conference, has served as Guest Editor of the IEEE Journal of Solid-State Circuits; and the International Journal of High Speed Electronics; and is currently an Associate Editor of JSSC.

He received the ISSCC Beatrice Winner Award for Editorial Excellence in 1994, the 1994 ISSCC and 1994 European Solid-State Circuits Conference Best Paper, and 1995 ISSCC Best Panel Awards.

He is the author of the book *Principles of Data Conversion System Design* (IEEE Press 1995) and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press 1996).

WILLY SANSEN

Willy Sansen has received the M.S. degree in Electrical Engineering from the Katholieke Universiteit Leuven in 1967 and the Ph.D in Electronics from the University of California, Berkeley, in 1972.

Since 1981 he has been full professor at the ESAT laboratory of the Katholieke Universiteit Leuven. During the period 1984-1990 he was the head of the Electrical Engineering Department.

He was Visiting Professor at Stanford University in 1978, at the Federal Technical University Lausanne in 1981, at the University of Pennsylvania Philadelphia in 1985 and at the Technical University Ulm in 1994.

He has been involved in design automation and numerous analog IC designs for telecommunications, consumer electronics, medical applications and sensors. He has supervised 30 Ph.D theses in the same field and authored and coauthored more than 300 papers in international journals and conference proceedings and six books, including the text (with K. Laker), *Design of Analog Integrated Circuits and Systems*.

ASHWIN SHAH

Ashwin Shah received the B. Tech degree in 1972 in Electrical Engineering from the Indian Institute of Technology, Bombay, and the M.S. degree in Electrical Engineering from the Illinois Institute of Technology, Chicago, in 1974.

He entered semiconductors in 1974 with Mostek Corporation in Carrollton, Texas as a design engineer. He first worked on an experimental SOS static RAM and later moved to the revolutionary 4k RAM design project. He joined Texas Instruments in 1975.

At TI Ashwin started on an MNOS-based non-volatile memory design and then in 1976 moved on to become the lead designer on the 64k CCD memory device. In 1980, he joined the R&D activity at TI as Member of the Technical Staff. At the same time, he also became lead designer for the VHSIC program sponsored by the U.S. Department of Defense. Based on his technical contributions, he was elected a Senior Member of the Technical Staff by his peers in 1983. His leading work on an experimental 4M DRAM received the 1986 ISSCC Best Paper Award. With the urge to learn something new, he started on the design of BiCMOS static RAM and ASICs. He directed the development teams for a high-performance 256k SRAM and 100k-gate ASIC. During this time he also managed a small team working on the silicon compilers for automatic filter implementation in BiCMOS arrays. In 1988 he was elected TI Fellow by his peers.

In 1989 he moved into technical management as the Associate Director of the VLSI Design Laboratory, and was later appointed the Director of the Scaled Technology Integration Laboratory, and in 1993 Director of the Semiconductor Process & Device Center. In 1994 he was appointed Vice President, Semiconductor Group.

He has been active with the IEEE since the mid-80s. He was a member of the Program Committee of ISSCC from 1987-1992 and Program Chairman in 1992. He has also been a Program Committee member of the Symposium on VLSI Circuits. He was a Guest Editor of the JSSC in 1988. He has authored or co-authored 34 publications and 23 patents. He was elected IEEE Fellow in 1996.

ERIC VITTOZ

Eric Vittoz was born in Lausanne, Switzerland on May 9, 1938. He received the M.S. and Ph.D degrees in Electrical Engineering from the Swiss Federal Institute of Technology in Lausanne (EPFL), in 1961 and 1969, respectively.

After spending one year as a research assistant, he joined the Centre Electronique Horloger S.A., Neuchâtel, in 1962,

where he became involved in micropower integrated circuit development for watches, while working on his thesis in the same field. In 1971 he was appointed Vice Director, supervising advanced development in electronic watches and other micropower systems. In 1984, he took the responsibility for the Circuits and Systems Research Division of the Swiss Center for Electronics and Microtechnology (CSEM) in Neuchâtel, where he was appointed Executive Vice President, Integrated Circuits and Systems, from 1991 to 1995. Since 1996, he has been a Senior Vice President heading the Bio-inspired System Section of CSEM. His research interest is design of low-power analog CMOS circuits, with present emphasis on application to analog VLSI for perceptive computation. Since 1975, he has lectured and supervised student projects in analog circuit design at EPFL, where he became Professor in 1982.

He has been a member of the ISSCC European Program Committee more than 10 years, European representative on the Solid-State Circuits Council for two years, and is a member of the Steering Committee of the European Solid-State Circuits Conference. He was elected IEEE Fellow in 1989.

BRUCE WOOLEY

Bruce Wooley is a Professor of Electrical Engineering and the Director of the Integrated Circuits Laboratory at Stanford University. He received the B.S., M.S., and Ph.D degrees in Electrical Engineering from the University of California, Berkeley, in 1966, 1968, and 1970, respectively.

From 1970 to 1984 he was a member of the research staff at Bell Laboratories, Holmdel, NJ. He joined Stanford University in 1984. His research is in the field of integrated circuit design, where his interests include over-sampling A/D and D/A conversion, low-power mixed-signal design, high-speed embedded memory, high-performance packaging and testing, noise in mixed-signal integrated circuits, circuit design techniques for video and image data acquisition, and circuits for wireless communications.

He is an IEEE Fellow, and has served as Editor of the IEEE Journal of Solid-State Circuits and as Chairman of both the ISSCC and the Symposium on VLSI Circuits. He is a past Chairman of the IEEE Solid-State Circuits and Technology Committee and served as a member of the IEEE Solid-State Circuits Council, the Executive Committee of ISSCC and the IEEE Circuits and Systems AdCom. He currently chairs the Publications Committee of the Solid-State Circuits Council, and is a member of the Executive Committee for the Symposium on VLSI Circuits.

He has published more than 100 technical articles and is the co-editor of *Analog MOS Integrated Circuits II*.

ISSCC News

John Trnka

trnka@vnet.ibm.com

CDROM Update

CDROMs were shipped to all ISSCC'96 attendees the end of July. If you have not received your copy, please contact John Wuorinen at 207-326-8811 or FAX 207-326-8878. Be sure to install the Adobe program from the CD for viewing the ISSCC CDROM, even if you already have Adobe on your system. There are a number of unique support files that must be installed in order to properly view this CDROM. If you have comments related to improvements to future CDROMs, please contact Tim Tredwell at 716-477-4329 or tredwell@kodak.com.

Growing Pains!

The large increase in both conference attendance and total sessions this past year resulted in some inconvenience to attendees. These issues are being addressed by the conference Executive Committee and its Vision Committee for the '97 Conference. Work is underway to streamline registration, particularly for the Workshop and Tutorials, by providing confirmation of registration to attendees enrolled in either the Workshop or the Tutorials.

Web Site

There is a considerable amount of up-to-date information available about ISSCC at its WEB site. The following items are available on the WEB: activities calendar, author information including information on manuscript preparation, and a complete listing of committees related to ISSCC. Copies of Advance Programs from the past two years are also available. Look for the program for ISSCC'97 to be available in November, along with registration information.

The ISSCC WEB site is available at <http://www.isscc.org/>. Note: occasional problems have occurred with this address; work is underway to understand the problems. If you are experiencing problems, try the direct address: http://www_scc.eecg.toronto.edu/isscc/.

1997 ISSCC Call for Papers

Original papers are solicited in subject areas including but not limited to analog, communications, digital, memory, sensors, imagers, displays, signal processing, and technology directions.

Conference Theme

The 1997 Conference theme is *Multimedia*. Papers targeting multimedia applications in all the above areas are encouraged. Examples of IC technology are imagers, mixed-signal signal processing circuits, audio and video compression circuits, digital communications and display interfaces. Examples of application areas are computer education and games, desktop conferencing, set-top boxes and video-on-demand systems.

New Guidelines for the Preliminary Version of the Paper, Abstract and Supplementary Material

To improve efficiency of the paper selection process, and to better match the defacto submissions received, changes have been implemented in the paper submission process.

Authors should submit three items for review:

- A draft of the final manuscript
- An abstract for the advance program
- Supplementary material.

The draft text must not exceed 110 65-character lines. Six figures are allowed in addition to a die photograph. All authors of accepted papers will have an opportunity to revise their draft. The ISSCC Program Committee may require revisions incorporating its recommendations.

The abstract must not exceed five 65-character lines. It may be edited without consultation to accommodate the program format. It must be factual and provide as complete a description as possible, including specific performance data. Please refer to past Advance Programs for examples. Marketing claims, such as "new," "advanced," "novel," "high performance," and "high speed" should be avoided.

Supplementary material should be supplied as an attachment to, but separate from, the draft manuscript. This material should contain information that will help the program committee in its decisions. Examples are copies of additional figures to be shown as slides, additional text explaining key points in more detail, and a clear review of how the work described extends the previous state of the art. Successful submissions must contain specific new results, sufficient detail and data to be understood, and schematics and measured results for key circuits when appropriate. Supplementary material must also state clearly what, if anything, will have been published prior to the conference. Copies of these prior publications should be included. Please include data sheets, press releases, and other forms of publication.

ISSCC Paper Submission

RECEIPT DEADLINE: FRIDAY, SEPT. 6, 1996

ALL AUTHORS must forward 30 copies of the preliminary version of the paper, abstract, and supplementary material for receipt by the deadline to:

John Wuorinen
2 School Street
Castine, ME 04421-0304, USA

Tel.: 207-326-8811 Fax: 207-326-8878

email: 71762.2626@compuserve.com

A EUROPEAN AUTHOR should, in addition, send 20 copies of the preliminary version of the paper, abstract, and supplementary material to:

Willy Sansen
Katholieke Univ. Leuven,
Elektrotechniek-ESAT-MICAS
94 Kardinaal Mercierlaan
B-3001 Leuven, Belgium

Tel.: 32-16-32-10-78 Fax: 32-16-32-19-75

email: willy.sansen@esat.kuleuven.ac.be

A FAR-EAST AUTHOR should, in addition, send 20 copies of the preliminary version of the paper, abstract, and supplementary material to:

Katsuhiko Shimohigashi
Hitachi Ltd., Semiconductor Development Center.
Semiconductor, & IC Division
1-280 Higashi-Koigakubo
Kokubunji, Tokyo 185, Japan

Tel.: 81-423-23-1111 x4300 Fax: 81-423-27-7847

email: k-shimoh@crl.hitachi.co.jp

Other Contacts

For further details on pre-publication policy, or assistance in assigning a subject area, contact the Program Committee Chair: Dick Hester, Texas Instruments,
Tel: 214-995-7102, Fax: 214-995-6194
email: hester@hc.ti.com

For further details on manuscript preparation, contact the Digest Editor, John Wuorinen,
Tel: 207-326-8811 Fax: 207-326-8878,
email: 71762.2626@compuserve.com

Press Relations are handled by:

Kenneth C. Smith
Hong Kong Univ. of Sci. & Tech., Dept. of EE,
Clear Water Bay
Kowloon, Hong Kong

Tel: +852-2358-7062 Fax: +852-2335-0194

email: eesmith@ee.ust.hk

Conference Operations are handled by:

Diane Suiters
Courtesy Associates
655 Fifteenth St, NW, Suite 300
Washington, DC 20005, USA.

Tel. 202-639-4255 Fax: 202-347-6109

email: isscc@mcimail.com

Call for Awards Nominations

Lew Terman

terman@watson.ibm.com

The Solid-State Circuits Council strongly urges nomination of members of the solid-state circuits community for IEEE awards and IEEE fellow grade membership. It is important to recognize outstanding accomplishments, yet no one can receive an award or be elevated to Fellow unless nominated. Nomination is straightforward; requiring submission of a nomination form with supporting letters. Completion of the nomination form with the help of the nominee is encouraged.

The IEEE Technical Field Awards are Institute-wide awards given for outstanding accomplishment in a specific technical area. **Solid-State Circuits Technical Field Awards** are given for "outstanding contributions in the field of solid-state circuits by an individual or team of not more than three." Previous recipients include Rudy van de Plassche, Paul Gray, Kiyoo Itoh, Toshi Masuhara, and Barrie Gilbert. Nominees need not be IEEE members. Other IEEE Technical Field Awards of relevance to solid-state circuits are Liebmann (emerging technologies), Brunetti (miniaturization), and Sarnoff (electronics). The deadline for receipt of Technical Field Award nominations is January 31, 1997.

IEEE Fellow, the highest IEEE membership grade, is granted in recognition of outstanding accomplishment as engineer/scientist, educator, or technical leader. A nominee must be a Senior Member at the time of the deadline for receipt of nominations, March 15, 1997.

Information and nomination kits may be obtained by contacting the SSCC Awards Chair or the IEEE:

Lewis Terman, SSCC Awards Chair
IBM Research Center
P.O. Box 218 M/S 25-251
Yorktown Hgts., NY 10598
Tel: (914) 945-2029, FAX: (914) 945-1358
terman@watson.ibm.com

IEEE Awards and Recognition
P.O. Box 1331
445 Hoes Lane
Piscataway, NJ 08855-1331
Tel: (908) 562-2840, FAX: (908) 981-9019
awards@ieee.org

IEEE Fellow Program
P.O. Box 1331
445 Hoes Lane
Piscataway, NJ 08855-1331
Tel: (908) 562-3843, FAX: (908) 981-9019
j.kilyk@ieee.org

World-Wide-WEB Update

John Trnka

trnka@vnet.ibm.com

The Solid-State Circuits Council (Society) is maintaining a home page on the World-Wide-WEB at http://www_ssc.eecg.toronto.edu/. This page can also be accessed from the "IEEE Technical Societies" reference on the IEEE home page <http://www.ieee.org/> and then selecting "Solid-State Circuits Council/Society."

A copy of this newsletter, as well as previous issues, can be viewed directly on the WEB by selecting the "Publications - Newsletter" from the SSCC homepage.

Information about the October SSCT Workshop has been updated and is available under "Meetings and Conferences - Council-Supported." In addition, a section containing the index to recent issues of the Journal of Solid-State Circuits is also available in the "Publications - JSSC" reference.

Links to the IEEE, ISSCC, and other Council supported events are also available on the Web through the SSCC Homepage.

Updates or additions to this home page can be requested from John Trnka at the above address.

Meetings Calendar

Charles G. Sodini

sodini@mit.edu

European Solid-State Circuits Conference
September 17-19, 1996 - Neuchâtel, Switzerland
Contact: Philippe Aubert 41-38-205-428

ASIC Conference
September 23-27, 1996 - Rochester, NY
Contact: Lynne Engelbrecht 716-254-2350

Workshop on Selected Topics in IC Design
September 30, 1996 - Dana Point, CA
Contact: Stan Schuster 914-945-1191

International Solid-State Circuits Conference
February 6-8, 1997 - San Francisco, CA
Contact: Diane Suiters 202-639-4255

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