Memristor—The Missing Circuit Element

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Abstract—A new two-terminal circuit element—called the *memristor*—characterized by a relationship between the *charge* $q(t) \equiv \int_{-\infty}^{t} i(\tau)\, d\tau$ and the *flux-linkage* $\varphi(t) \equiv \int_{-\infty}^{t} v(\tau)\, d\tau$ is introduced as the *fourth basic* circuit element. An electromagnetic field interpretation of this relationship in terms of a quasi-static expansion of Maxwell's equations is presented. Many circuit-theoretic properties of memristors are derived. It is shown that this element exhibits some peculiar behavior different from that exhibited by resistors, inductors, or capacitors. These properties lead to a number of unique applications which cannot be realized with *RLC* networks alone.

Although a physical memristor device without internal power supply has not yet been discovered, operational laboratory models have been built with the help of active circuits. Experimental results are presented to demonstrate the properties and potential applications of memristors.

I. Introduction

THIS PAPER presents the logical and scientific basis for the existence of a new two-terminal circuit element called the *memristor* (a contraction for *memory resistor*) which has every right to be as basic as the three classical circuit elements already in existence, namely, the resistor, inductor, and capacitor. Although the existence of a memristor in the form of a *physical device* without internal power supply has not yet been discovered, its laboratory realization in the form of active circuits will be presented in Section II.[1] Many interesting circuit-theoretic properties possessed by the memristor, the most important of which is perhaps the *passivity property* which provides the circuit-theoretic basis for its physical realizability, will be derived in Section III. An electromagnetic field interpretation of the memristor characterization will be presented in Section IV with the help of a quasi-static expansion of Maxwell's equations. Finally, some novel applications of memristors will be presented in Section V.

II. Memristor—The Fourth Basic Circuit Element

From the circuit-theoretic point of view, the three basic two-terminal circuit elements are defined in terms of a *relationship* between two of the four fundamental circuit variables, namely, the *current* i, the *voltage* v, the *charge* q, and the *flux-linkage* φ. Out of the *six* possible combinations of these four variables, five have led to well-known relationships [1]. Two of these relationships are already given by $q(t)=\int_{-\infty}^{t} i(\tau)\, d\tau$ and $\varphi(t)=\int_{-\infty}^{t} v(\tau)\, d\tau$. Three other relationships are given, respectively, by the *axiomatic* definition of the three classical circuit elements, namely, the *resistor* (defined by a relationship between v and i), the *inductor* (defined by a relationship between φ and i), and the *capacitor* (defined by a relationship between q and v). Only one relationship remains undefined, the relationship between φ and q. From the logical as well as axiomatic points of view, it is necessary for the sake of *completeness* to postulate the existence of a fourth basic two-terminal circuit element which

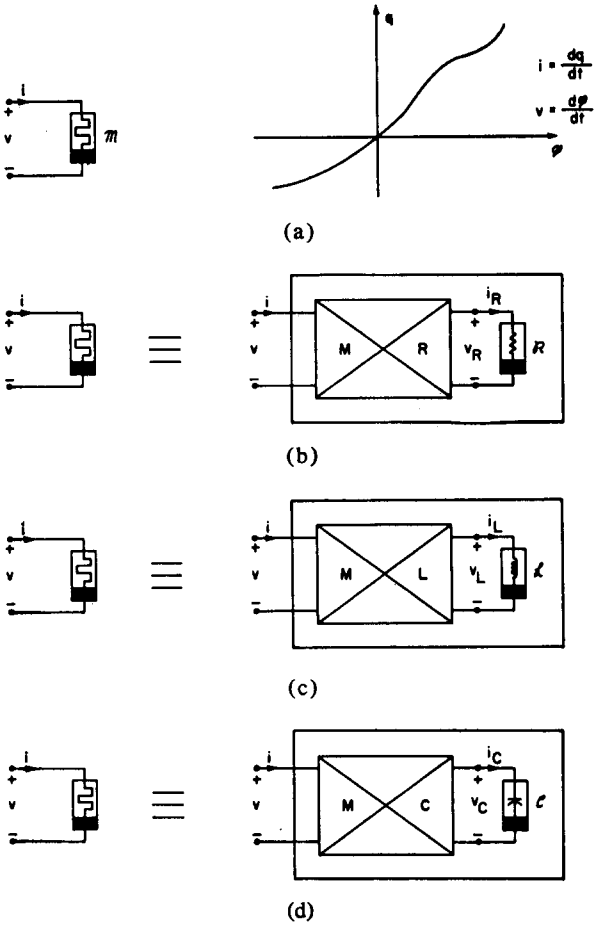

Fig. 1. Proposed symbol for memristor and its three basic realizations. (a) Memristor and its φ–q curve. (b) Memristor basic realization 1: M–R mutator terminated by nonlinear resistor $\mathcal{R}$. (c) Memristor basic realization 2: M–L mutator terminated by nonlinear inductor $\mathcal{L}$. (d) Memristor basic realization 3: M–C mutator terminated by nonlinear capacitor $\mathcal{C}$.

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[1] In a private communication shortly before this paper went into press, the author learned from Professor P. Penfield, Jr., that he and his colleagues at M.I.T. have also been using the memristor for modeling certain characteristics of the varactor diode and the partial superconductor. However, a physical device which corresponds exactly to a memristor has yet to be discovered.

TABLE I

CHARACTERIZATION AND REALIZATION OF *M–R*, *M–L*, AND *M–C* MUTATORS

	TYPE	SYMBOL AND CHARACTERIZATION	TRANSMISSION MATRIX $\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} T(p) \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$	BASIC REALIZATIONS USING CONTROLLED SOURCES	
M - R MUTATOR	1	$(q,\varphi) \longleftrightarrow (i_R, v_R)$ $v_1 = \frac{dv_2}{dt}$ $i_1 = -\frac{di_2}{dt}$	$T_{MR_1}(p) = \begin{bmatrix} p & 0 \\ 0 & p \end{bmatrix}$	REALIZATION 1	REALIZATION 2
	2	$(q,\varphi) \longleftrightarrow (v_R, i_R)$ $v_1 = -\frac{di_2}{dt}$ $i_1 = \frac{dv_2}{dt}$	$T_{MR_2}(p) = \begin{bmatrix} 0 & p \\ p & 0 \end{bmatrix}$	REALIZATION 1	REALIZATION 2
M - L MUTATOR	1	$(q,\varphi) \longleftrightarrow (i_L, \varphi_L)$ $v_1 = v_2$ $i_1 = -\frac{di_2}{dt}$	$T_{ML_1}(p) = \begin{bmatrix} 1 & 0 \\ 0 & p \end{bmatrix}$ (Identical to $T_{CR_1}(p)$ of a Type 1 C-R MUTATOR)	REALIZATION 1 REALIZATION 3	REALIZATION 2 REALIZATION 4
	2	$(q,\varphi) \longleftrightarrow (\varphi_L, i_L)$ $v_1 = -\frac{di_2}{dt}$ $i_1 = v_2$	$T_{ML_2}(p) = \begin{bmatrix} 0 & p \\ 1 & 0 \end{bmatrix}$ (Identical to $T_{LR_2}(p)$ of a Type 2 L-R MUTATOR)	REALIZATION 1	REALIZATION 2
M - C MUTATOR	1	$(q,\varphi) \longleftrightarrow (q_C, v_C)$ $v_1 = \frac{dv_2}{dt}$ $i_1 = -i_2$	$T_{MC_1}(p) = \begin{bmatrix} p & 0 \\ 0 & 1 \end{bmatrix}$ (Identical to $T_{LR_1}(p)$ of a Type 1 L-R MUTATOR)	REALIZATION 1 REALIZATION 3	REALIZATION 2 REALIZATION 4
	2	$(q,\varphi) \longleftrightarrow (v_C, q_C)$ $v_1 = -i_2$ $i_1 = \frac{dv_2}{dt}$	$T_{MC_2}(p) = \begin{bmatrix} 0 & 1 \\ p & 0 \end{bmatrix}$ (Identical to $T_{CR_2}(p)$ of a Type 2 C-R MUTATOR)	REALIZATION 1	REALIZATION 2

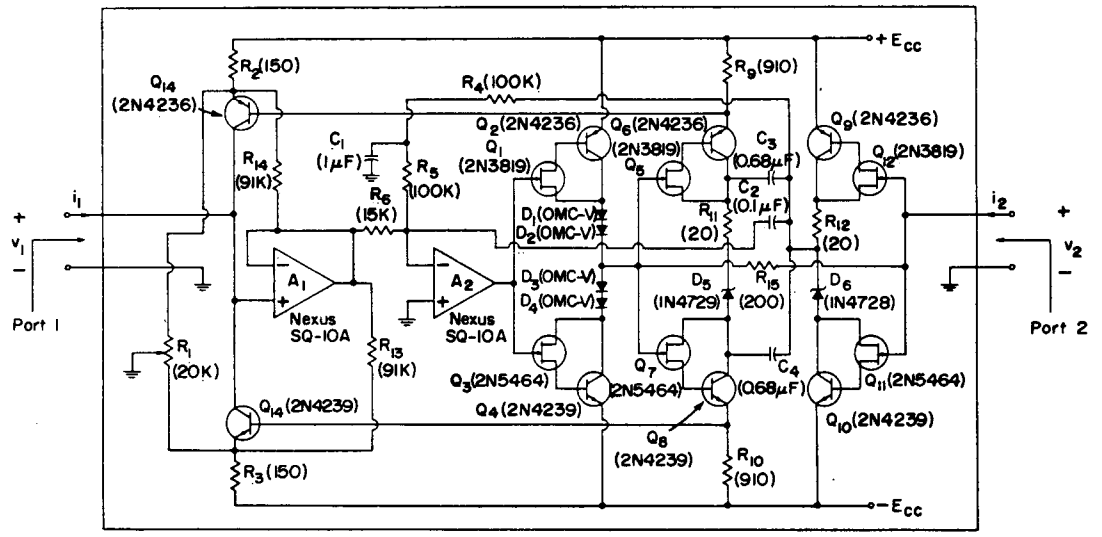

Fig. 2. Practical active circuit realization of type-1 M–R mutator based on realization 1 of Table I.

is characterized by a φ–q curve.[2] This element will henceforth be called the *memristor* because, as will be shown later, it behaves somewhat like a nonlinear resistor with memory.

The proposed symbol of a memristor and a hypothetical φ–q curve are shown in Fig. 1(a). Using a mutator [3], a memristor with any prescribed φ–q curve can be realized by connecting an appropriate nonlinear resistor, inductor, or capacitor across port 2 of an M–R mutator, an M–L mutator, and an M–C mutator, as shown in Fig. 1(b), (c), and (d), respectively. These mutators, of which there are two types of each, are defined and characterized in Table I.[3] Hence, a type-1 M–R mutator would transform the v_R–i_R curve of the nonlinear resistor $f(v_R, i_R)=0$ into the corresponding φ–q curve $f(\varphi, q)=0$ of a memristor. In contrast to this, a type-2 M–R mutator would transform the i_R–v_R curve of the nonlinear resistor $f(i_R, v_R)=0$ into the corresponding φ–q curve $f(\varphi, q)=0$ of a memristor. An analogous transformation is realized with an M–L mutator (M–C mutator) with respect to the (φ_L, i_L) or (i_L, φ_L) $[(v_C, q_C)$ or $(q_C, v_C)]$ curve of a nonlinear inductor (capacitor).

Each of the mutators shown in Table I can be realized by a two-port active network containing either one or two controlled sources, as shown by the various realizations in Table I. Since it is easier to synthesize a nonlinear resistor with a prescribed v–i curve [1], only operational models of M–R mutators have been built. A typical *active circuit realization* based on realization 1 (Table I) of a type-1 M–R mutator is given in Fig. 2. In order to verify that a memristor is indeed realized across port 1 of an M–R mutator when a nonlinear resistor is connected across port 2, it would be necessary to design a φ–q *curve tracer*. The complete schematic diagram of a practical φ–q curve tracer is shown in Fig. 3.[4] Using this tracer, the φ–q curves of three memristors realized by the type-1 M–R mutator circuit of Fig. 2 are shown in Fig. 4(b), (d), and (f) corresponding to the nonlinear resistor V–I curve shown in Fig. 4(c), (e), and (g), respectively. To demonstrate the rather "peculiar" voltage and current waveforms generated by the simple memristor circuit shown in Fig. 5(a), three representative memristors were synthesized with φ–q curves as shown in Fig. 5(b), (d), and (f), respectively. The oscilloscope tracings of the voltage $v(t)$ and current $i(t)$ of each memristor are shown in Fig. 5(c), (e), and (g), respectively. The waveforms in Fig. 5(c) and (e) are measured with a 63-Hz sinusoidal input signal, while the waveforms shown in Fig. 5(g) are measured with a 63-Hz triangular input signal. It is interesting to observe that these waveforms are rather peculiar in spite of the fact that the φ–q curve of the three memristors are relatively smooth. It should not be surprising, therefore, for us to find that the memristor possesses certain unique signal-processing properties not shared by any of the three existing classical elements. In fact, it is precisely these properties that have led us to believe that memristors will play an important role in circuit theory, especially in the area of device modeling and unconventional signal-processing applications. Some of these applications will be presented in Section V.

III. Circuit-Theoretic Properties of Memristors

By definition a memristor is characterized by a *relation* of the type $g(\varphi, q)=0$. It is said to be charge-controlled (flux-controlled) if this relation can be expressed as a single-valued function of the charge q (flux-linkage φ). The voltage

[2] The postulation of new elements for the purpose of completeness of a physical system is not without scientific precedent. Indeed, the celebrated discovery of the periodic table for chemical elements by Mendeleeff in 1869 is a case in point [2].

[3] Observe that a type-1 (type-2) M–L mutator is identical to a type-1 (type-2) C–R mutator (L–R mutator). Similarly, a type-1 (type-2) M–C mutator is identical to a type-1 (type-2) L–R mutator (C–R mutator).

[4] For additional details concerning the design and operational characteristics of the circuits shown in Figs. 2 and 3, as well as that for a type-2 M–R mutator, see [4].

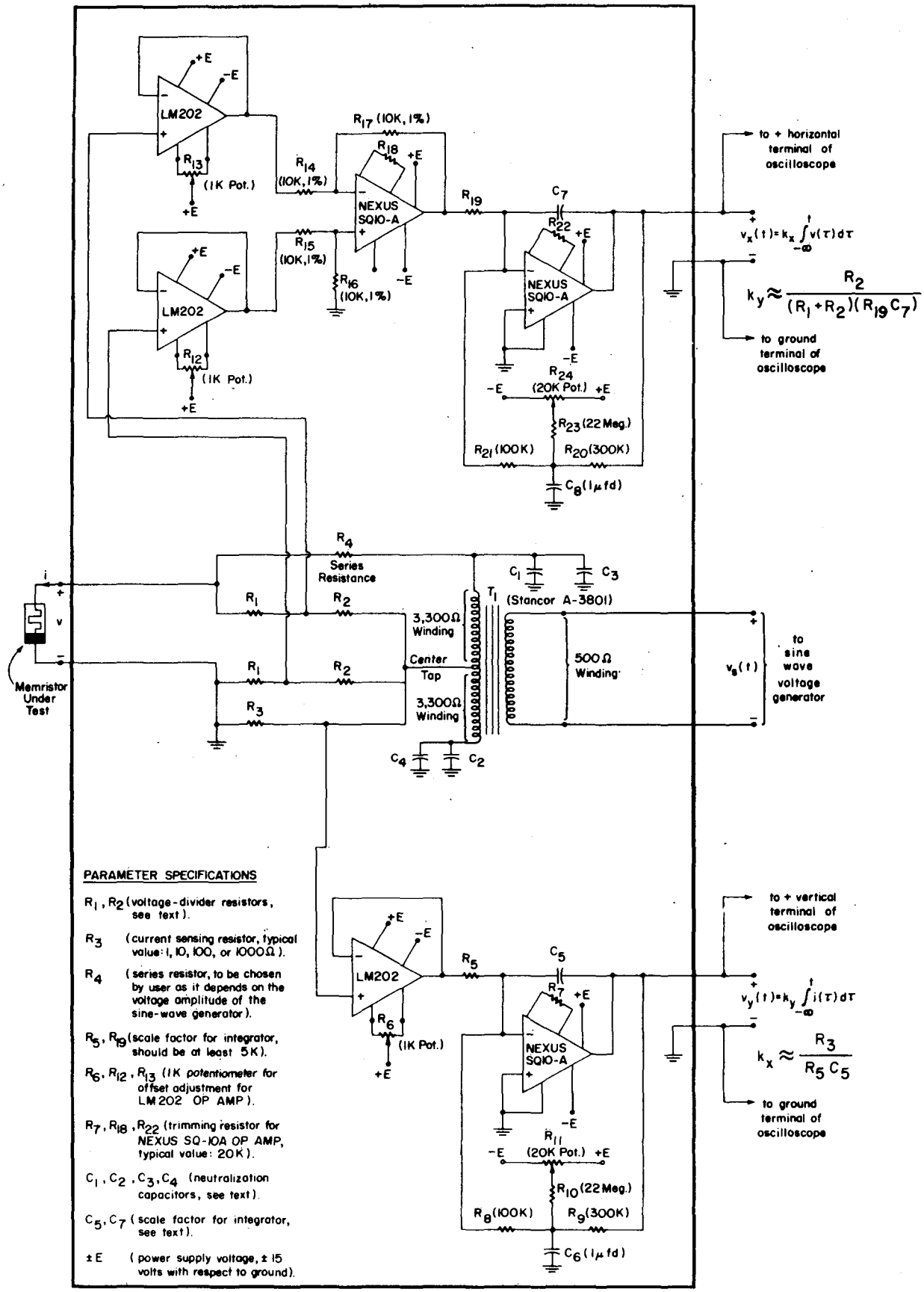

Fig. 3. Complete schematic diagram of memristor tracer for tracing the φ–q curve of a memristor.

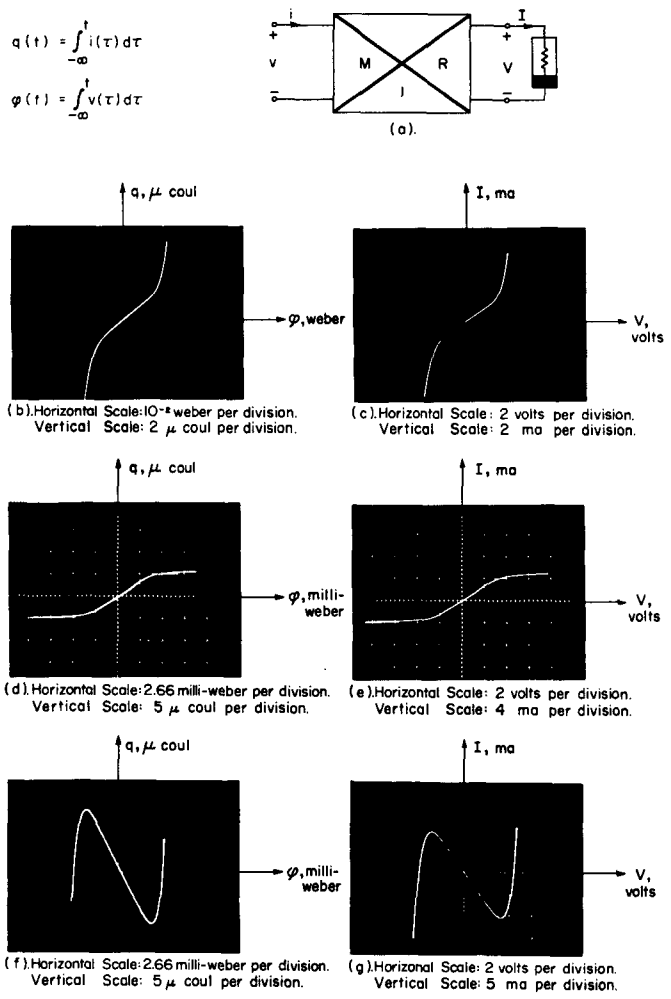

Fig. 4. φ–q curves of three typical memristors.

across a charge-controlled memristor is given by

$$v(t) = M(q(t))i(t) \tag{1}$$

where

$$M(q) \equiv d\varphi(q)/dq \tag{2}$$

Similarly, the current of a flux-controlled memristor is given by

$$i(t) = W(\varphi(t))v(t) \tag{3}$$

where

$$W(\varphi) \equiv dq(\varphi)/d\varphi \tag{4}$$

Since $M(q)$ has the unit of resistance, it will henceforth be called the *incremental memristance*. In contrast to this, the function $W(\varphi)$ will henceforth be called the *incremental menductance* because it has the unit of a conductance. Observe that the value of the incremental memristance (memductance) at any time t_0 depends upon the time integral of the memristor current (voltage) from $t=-\infty$ to $t=t_0$. Hence, while the memristor behaves like an ordinary resistor at a given instant of time t_0, its resistance (conductance) depends on the complete past history of the memristor current (voltage). This observation justifies our choice of the name memory resistor, or memristor. It is interesting to observe that once the memristor voltage $v(t)$ or current $i(t)$ is specified, the memristor behaves like a *linear time-varying resistor*. In the very special case where the memristor φ–q curve is a straight line, we obtain $M(q)=R$, or $W(\varphi)=G$, and the memristor reduces to a *linear time-invariant resistor*. Hence, there is no point introducing a linear memristor in linear network theory.[5]

We have already shown that memristors with almost any φ–q curve can be synthesized in practice by active networks. The following passivity criterion shows what class of memristors might be discovered in a pure "device form" without internal power supplies.

Theorem 1: Passivity Criterion

A memristor characterized by a differentiable charge-controlled φ–q curve is passive if, and only if, its incremental memristance $M(q)$ is nonnegative; i.e., $M(q)\geq 0$.

Proof: The instantaneous power dissipated by a memristor is given by

$$p(t) = v(t)i(t) = M(q(t))[i(t)]^2. \tag{5}$$

Hence, if the incremental memristance $M(q)\geq 0$, then $p(t)\geq 0$ and the memristor is obviously passive. To prove the converse, suppose that there exists a point q_0 such that $M(q_0)<0$. Then the differentiability of the φ–q curve implies that there exists an $\epsilon>0$ such that $M(q_0+\Delta q)<0$, $|\Delta q|<\epsilon$. Now let us drive the memristor with a current $i(t)$ which is zero for $t\leq \hat{t}$ and such that $q(t)=q_0+\Delta q(t)$ for $t\geq t_0\geq \hat{t}$ where $|\Delta q(t)|<\epsilon$; then $\int_{-\infty}^{t} p(\tau)\,d\tau<0$ for sufficiently large t, and hence the memristor is active. Q.E.D.

We remark that the above criterion remains valid if the "differentiability" condition is replaced by a "continuity" condition, provided that the left- and right-hand derivative at each point on the φ–q curve exists. This criterion shows that only memristors characterized by a *monotonically increasing* φ–q curve can exist in a device form without internal power supplies. We also remark that except possibly for some pathological φ–q curves,[6] a passive memristor does not seem to violate any known physical laws.

[5] Since research in circuit theory in the past has been dominated by linear networks, it is not surprising that the concept of a memristor never arose there. Neither is it surprising that this element is not even yet discovered in a device form because it is somewhat "unnatural" to associate charge with flux-linkage. Moreover, the necessity to design a φ–q curve tracer all but eliminates the slim possibility of an accidental discovery.

[6] It is possible for a passive circuit element to violate the second law of thermodynamics. For a thought-provoking exposition on this topic, see [5].

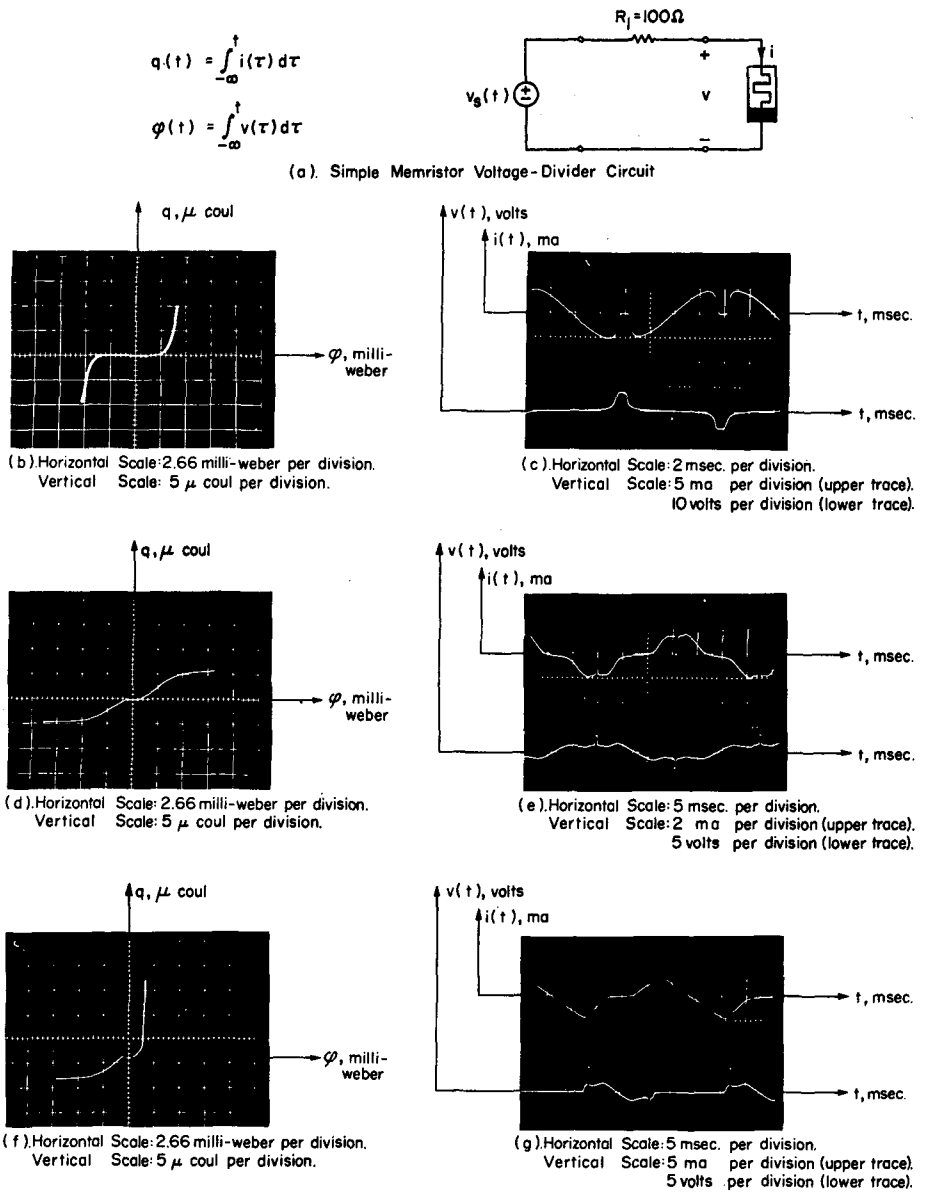

Fig. 5. Voltage and current waveforms associated with simple memristor circuit corresponding to a sinusoidal input signal [(c) and (e)] and a triangular input signal [(g)], respectively.

Theorem 2: Closure Theorem

A one-port containing only memristors is equivalent to a memristor.

Proof: If we let i_j, v_j, q_j, and φ_j denote the current, voltage, charge, and flux-linkage of the jth memristor, where $j=1, 2, \cdots, b$, and if we let i and v denote the port current and port voltage of the one-port, then we can write $(n-1)$ independent KCL (Kirchhoff current law) equations (assuming the network is connected); namely,

$$\alpha_{j0} i + \sum_{k=1}^{b} \alpha_{jk} i_k = 0, \qquad j = 1, 2, \cdots, n-1 \tag{6}$$

where α_{jk} is either 1, −1, or 0, b is the total number of memristors, and n is the total number of nodes. Similarly, we can write a system of $(b-n+2)$ independent KVL (Kirchhoff voltage law) equations:

$$\beta_{j0} v + \sum_{k=1}^{b} \beta_{jk} v_k = 0, \qquad j = 1, 2, \cdots, b-n+2 \tag{7}$$

where β_{jk} is either 1, −1, or 0. If we integrate each equation in (6) and (7) with respect to time and then substitute $\varphi_k = \varphi_k(q_k)$ for φ_k in the resulting expressions,[7] we obtain

$$\sum_{k=1}^{b} \alpha_{jk} q_k = Q_j - \alpha_{j0} q, \qquad j = 1, 2, \cdots, n-1 \tag{8}$$

$$\beta_{j0} \varphi + \sum_{k=1}^{b} \beta_{jk} \varphi_k(q_k) = \Phi_j, \quad j = 1, 2, \cdots, b-n+2 \tag{9}$$

[7] We have assumed for simplicity that the memristors are charge-controlled. The proof can be easily modified to allow memristors characterized by arbitrary φ–q curves.

where Q_j and Φ_j are arbitrary constants of integration. Equations (8) and (9) together constitute a system of $(b+1)$ independent nonlinear functional equations in $(b+1)$ unknowns. Hence, solving for φ, we obtain a *relation* $f(q, \varphi)=0$.

Q.E.D.

Theorem 3: Existence and Uniqueness Theorem[8]

Any network containing only memristors with positive incremental memristances has one, and only one, solution.

Proof: Since the governing equations of a network containing only memristors are identical in form to the governing equations of a network containing only nonlinear resistors, the proof follows *mutatis mutandis* the well-known proof given in [6], [7]. Q.E.D.

It is sometimes easier and more instructive to analyze a single-element-type nonlinear network by finding the stationary points of an associated scalar potential function [8], [9]. We will now present an analogous development of this concept for a pure memristor network.[9]

Definition 1

We define the *action* (*coaction*) associated with a charge-controlled (flux-controlled) memristor to be the integral

$$A(q)\equiv\int_0^q \varphi(q)\,dq \qquad (\hat{A}(\varphi)\equiv\int_0^\varphi q(\varphi)\,d\varphi).$$

Consider now a pure memristor network N containing n nodes and b branches. Let $\mathfrak{I}$ be a *tree* of N and $\mathfrak{L}$ its associated *cotree*. Let us label the branches consecutively starting with the tree elements and define $\boldsymbol{\varphi}=(\varphi_1, \varphi_2, \cdots, \varphi_b)^t$, $\boldsymbol{q}=(q_1, q_2, \cdots, q_b)^t$, $\boldsymbol{\varphi}_\mathfrak{I}=(\varphi_1, \varphi_2, \cdots, \varphi_{n-1})^t$, and $\boldsymbol{q}_\mathfrak{L}=(q_n, q_{n+1}, \cdots, q_b)^t$. It is well known that either $\boldsymbol{\varphi}_\mathfrak{I}$ or $\boldsymbol{q}_\mathfrak{L}$ constitutes a complete set of variables in the sense that $\boldsymbol{\varphi}=\boldsymbol{D}^t\boldsymbol{\varphi}_\mathfrak{I}$ and $\boldsymbol{q}=\boldsymbol{B}^t\boldsymbol{q}_\mathfrak{L}$, where $\boldsymbol{D}$ and $\boldsymbol{B}$ are the *fundamental cut-set matrix* and the *fundamental loop matrix*, respectively [10].

Definition 2

We define the total action $\mathfrak{A}(\boldsymbol{q}_\mathfrak{L})$ [total coaction $\hat{\mathfrak{A}}(\boldsymbol{\varphi}_\mathfrak{I})$] associated with a network N containing charge-controlled (flux-controlled) memristors to be the scalar function

$$\boxed{\mathfrak{A}(\boldsymbol{q}_\mathfrak{L}) = A \circ (\boldsymbol{B}^t\boldsymbol{q}_\mathfrak{L})} \qquad \boxed{\hat{\mathfrak{A}}(\boldsymbol{\varphi}_\mathfrak{I}) = \hat{A} \circ (\boldsymbol{D}^t\boldsymbol{\varphi}_\mathfrak{I})} \quad (10)$$

where

$$A = A(\boldsymbol{q}) = \sum_{j=1}^{b} A_j(q_j) = \sum_{j=1}^{b}\int_0^{q_j} \varphi_j(q_j)\,dq_j$$

$$\hat{A} = \hat{A}(\boldsymbol{\varphi}) = \sum_{j=1}^{b} \hat{A}_j(q_j) = \sum_{j=1}^{b}\int_0^{\varphi_j} q_j(\varphi_j)\,d\varphi_j \quad (11)$$

and where $\circ$ denotes the "composition" operation.

[8] To simplify the hypothesis, we assume that all memristors are characterized by differentiable onto functions.

[9] Several useful potential functions have been defined for the three classical circuit elements. They are the content and cocontent of a resistor [8], the *magnetic energy* and *magnetic coenergy* of an inductor [9], and the *electric energy* and *electric coenergy* of a capacitor [9].

Theorem 4: Principle of Stationary Action (*Coaction*)

A vector $\boldsymbol{q}_\mathfrak{L}=\boldsymbol{Q}_\mathfrak{L}$ ($\boldsymbol{\varphi}_\mathfrak{I}=\boldsymbol{\Phi}_\mathfrak{I}$) is a solution of a network N containing only charge-controlled (flux-controlled) memristors if, and only if, it is a *stationary point* of the total action $\mathfrak{A}(\boldsymbol{q}_\mathfrak{L})$ [total coaction $\mathfrak{A}(\boldsymbol{\varphi}_\mathfrak{I})$] associated with N; i.e., the gradient of $\mathfrak{A}(\boldsymbol{q}_\mathfrak{L})$ ($\hat{\mathfrak{A}}(\boldsymbol{\varphi}_\mathfrak{I})$) evaluated at $\boldsymbol{Q}_\mathfrak{L}$ ($\boldsymbol{\Phi}_\mathfrak{I}$) is zero:

$$\partial\mathfrak{A}(\boldsymbol{q}_\mathfrak{L})/\partial\boldsymbol{q}_\mathfrak{L}\,|_{\boldsymbol{q}_\mathfrak{L}=\boldsymbol{Q}_\mathfrak{L}} = \boldsymbol{0} \qquad \partial\hat{\mathfrak{A}}(\boldsymbol{\varphi}_\mathfrak{I})/\partial\boldsymbol{\varphi}_\mathfrak{I}\,|_{\boldsymbol{\varphi}_\mathfrak{I}=\boldsymbol{\Phi}_\mathfrak{I}} = \boldsymbol{0}. \quad (12)$$

Proof: It suffices to prove the charge-controlled case since the flux-controlled case will then follow by duality. Taking the gradient of $\mathfrak{A}(\boldsymbol{q}_\mathfrak{L})$ and applying the chain rule for differentiating composite functions, we obtain

$$\partial\mathfrak{A}(\boldsymbol{q}_\mathfrak{L})/\partial\boldsymbol{q}_\mathfrak{L} = \partial A \circ (\boldsymbol{B}^t\boldsymbol{q}_\mathfrak{L})/\partial\boldsymbol{q}_\mathfrak{L}$$
$$= \boldsymbol{B}\partial A(\boldsymbol{q})/\partial\boldsymbol{q}\,|_{\boldsymbol{q}=\boldsymbol{B}^t\boldsymbol{q}_\mathfrak{L}} = \boldsymbol{B}\boldsymbol{\varphi} \circ (\boldsymbol{B}^t\boldsymbol{q}_\mathfrak{L}). \quad (13)$$

But the expression $\boldsymbol{B}\boldsymbol{\varphi} \circ (\boldsymbol{B}^t\boldsymbol{q}_\mathfrak{L})=0$ since this is simply the set of KVL equations written in terms of $\mathfrak{L}$. Consequently, any vector $\boldsymbol{Q}_\mathfrak{L}$ is a solution of N if, and only if, it is a stationary point of $\mathfrak{A}(\boldsymbol{q}_\mathfrak{L})$. Q.E.D.

Since the action and coaction of a memristor is a potential function, they can be used to derive *frequency power formulas* for memristors operating as frequency converters. We assume the memristor is operating in the steady state so that we can write the following variables in multiply-periodic Fourier series:

$$v(t) = \mathrm{Re}\sum_\alpha [V_\alpha e^{j\omega_\alpha t}] \qquad i(t) = \mathrm{Re}\sum_\alpha [I_\alpha e^{j\omega_\alpha t}]$$

$$\varphi(t) = \mathrm{Re}\sum_\alpha [\Phi_\alpha e^{j\omega_\alpha t}] \qquad q(t) = \mathrm{Re}\sum_\alpha [Q_\alpha e^{j\omega_\alpha t}]$$

and

$$A(t)=\mathrm{Re}\sum_\alpha [A_\alpha e^{j\omega_\alpha t}]$$

where $V_\alpha \geq j\omega_\alpha\Phi_\alpha$ and $I_\alpha \geq j\omega_\alpha Q_\alpha$. Following identical procedure and notation as given in [11, ch. 3], we let ω_a denote the set of *independent* frequencies and make a small change in $\delta\phi_a\equiv\delta(\omega_a t)$. This perturbation induces a change in the action $A(t)$:

$$\delta A = \mathrm{Re}\sum_\alpha jA_\alpha(\partial\omega_\alpha/\partial\omega_a)e^{j\omega_\alpha t}\delta\phi_a. \quad (14)$$

But since $A(q)=\int_0^q\varphi(q)\,dq$, we have

$$\delta A = (\varphi)(\delta q) = \left[\mathrm{Re}\sum_\alpha \frac{V_\alpha}{j\omega_\alpha}e^{j\omega_\alpha t}\right] \cdot \left[\mathrm{Re}\sum_\alpha \frac{I_\alpha}{\omega_\alpha}(\partial\omega_\alpha/\partial\omega_a)e^{j\omega_\alpha t}\delta\phi_a\right]. \quad (15)$$

Equating (14) and (15) and taking their time averages, we obtain the following Manley–Rowe-like formula relating the *reactive powers* $\hat{P}_\alpha\equiv\frac{1}{2}\,\mathrm{Im}\,(V_\alpha I_\alpha^*)$:

$$\boxed{\sum_\alpha[\partial\omega_\alpha/\partial\omega_a][\hat{P}_\alpha/\omega_\alpha^2] = 0} \quad . \quad (16)$$

It is possible to derive a Page–Pantell-like inequality relating the *real powers* of a passive memristor by making use of the passivity criterion $(\delta\varphi)(\delta q)\geq 0$ (Theorem 1); namely,

$$\boxed{\sum_{\alpha} [\partial\omega_\alpha/\partial\omega_a]^2 [P_\alpha/\omega_\alpha^2] \geq 0} \tag{17}$$

where $P_\alpha \equiv \frac{1}{2}$ Re $(V_\alpha I_\alpha^*)$ is the *real power* at frequency ω_α. Since the procedure for deriving (17) follows again *mutatis mutandis* that given by Penfield [11], it will not be given here to conserve space. An examination of (17) shows that gain proportional to the frequency squared is likely in a memristor upconverter, but that severe loss is to be expected in a memristor mixer. It is also easy to show that converting efficiencies approaching 100 percent may be possible in a memristor harmonic generator.

So far we have considered only pure memristor networks. Let us now consider the general case of a network containing resistors, inductors, capacitors, and memristors. The equations of motion for this class of networks now take the form of a system of m first-order nonlinear differential equations in the normal form $\dot{x}=f(x, t)$ [1], where x is an $m\times 1$ vector whose components are the state variables. The number m is called the "order of complexity" of the network and is equal to the maximum number of independent initial conditions that can be arbitrarily specified [1]. The following theorem shows how the order of complexity can be determined by inspection.

Theorem 5: Order of Complexity

Let N be a network containing resistors, inductors, capacitors, memristors, independent voltage sources, and independent current sources. Then the order of complexity m of N is given by

$$\boxed{\begin{aligned} m = (b_L + b_C + b_M) - (n_M + n_{CE} + n_{LM}) \\ - (\hat{n}_M + \hat{n}_{LJ} + \hat{n}_{CM}) \end{aligned}} \tag{18}$$

where b_L is the total number of inductors; b_C is the total number of capacitors; b_M is the total number of memristors; n_M is the number of independent loops containing only memristors; n_{CE} is the number of independent loops containing only capacitors and voltage sources; n_{LM} is the number of independent loops containing only inductors and memristors; $\hat{n}_M$ is the number of independent cut sets containing only memristors; $\hat{n}_{LJ}$ is the number of independent cut sets containing only inductors and current sources; $\hat{n}_{CM}$ is the number of independent cut sets containing only capacitors and memristors.

Proof: It is well known that the order of complexity of an *RLC* network is given by $m=(b_L+b_C)-n_{CE}-\hat{n}_{LJ}$ [1]. It follows, therefore, from (1)–(4) that for an *RLC*-memristor network with $n_m=n_{LM}=\hat{n}_M=\hat{n}_{CM}=0$, each memristor introduces a new state variable and we have $m=(b_L+b_C+b_M)-n_{CE}-\hat{n}_{LJ}$. Observe next that a *constraint* among the state variables occurs whenever an independent loop consisting of elements corresponding to those specified in the definition of n_M and n_{LM} is present in the network. [We assume the algebraic sum of charges around any loop (flux-linkages in any cut set) is zero.] Similarly, a constraint among the state variables occurs whenever an independent cut set consisting of elements corresponding to those specified in the definition of $\hat{n}_M$ and $\hat{n}_{CM}$ is present in the network. Since each constraint removes one degree of freedom each time this situation occurs, the maximum order of complexity $(b_L+b_C+b_M)$ must be reduced by one. Q.E.D.

IV. An Electromagnetic Interpretation of Memristor Characterization

It is well known that circuit theory is a limiting special case of electromagnetic field theory. In particular, the characterization of the three classical circuit elements can be given an elegant electromagnetic interpretation in terms of the *quasi-static* expansion of Maxwell's equations [12]. Our objective in this section is to give an analogous interpretation for the characterization of memristors. While this interpretation does not prove the physical realizability of a "memristor device" *without internal power supply*, it does suggest the strong plausiblity that such a device might someday be discovered. Let us begin by writing down Maxwell's equations in differential form:

$$\text{curl } \boldsymbol{E} = -\frac{\partial \boldsymbol{B}}{\partial t} \tag{19}$$

$$\text{curl } \boldsymbol{H} = J + \frac{\partial \boldsymbol{D}}{\partial t} \tag{20}$$

where $\boldsymbol{E}$ and $\boldsymbol{H}$ are the electric and magnetic field intensity, $\boldsymbol{D}$ and $\boldsymbol{B}$ are the electric and magnetic flux density, and J is the current density. We will follow the approach presented in [12] by defining a "family time" $\tau=\alpha t$, where α is called the "time-rate parameter." In terms of the new variable τ, Maxwell's equations become

$$\text{curl } \boldsymbol{E} = -\alpha\frac{\partial \boldsymbol{B}}{\partial \tau} \tag{21}$$

$$\text{curl } \boldsymbol{H} = J + \alpha\frac{\partial \boldsymbol{D}}{\partial \tau} \tag{22}$$

where $\boldsymbol{E}$, $\boldsymbol{H}$, $\boldsymbol{D}$, $\boldsymbol{B}$, and J are functions of not only the position (x, y, z), but also of α and τ. If we were to expand these vector quantities as a *formal* power series in α and substitute them into (21) and (22), we would obtain upon equating the coefficients of α^n, the *n*th-*order Maxwell's equations*, where $n=0, 1, 2, \cdots$.

Many electromagnetic phenomena and systems can be satisfactorily analyzed by using only the zero-order and first-order Maxwell's equations; the corresponding solutions are called *quasi-static fields*. It has been shown that circuit theory belongs to the realm of quasi-static fields and can be studied with the help of the following Maxwell's equations in quasi-static form [12].

Zero-Order Maxwell's Equations

$$\text{curl } \boldsymbol{E}_0 = \boldsymbol{0} \tag{23}$$

$$\text{curl } \boldsymbol{H}_0 = \boldsymbol{J}_0. \tag{24}$$

First-Order Maxwell's Equations

$$\text{curl } \boldsymbol{E}_1 = -\frac{\partial \boldsymbol{B}_0}{\partial \tau} \tag{25}$$

$$\text{curl } \boldsymbol{H}_1 = \boldsymbol{J}_1 + \frac{\partial \boldsymbol{D}_0}{\partial \tau}. \tag{26}$$

The total quasi-static vector quantities are obtained by keeping only the first two terms of the formal power series and by setting $\alpha = 1$; namely, $\boldsymbol{E} \approx \boldsymbol{E}_0 + \boldsymbol{E}_1$, $\boldsymbol{H} \approx \boldsymbol{H}_0 + \boldsymbol{H}_1$, $\boldsymbol{D} \approx \boldsymbol{D}_0 + \boldsymbol{D}_1$, $\boldsymbol{B} \approx \boldsymbol{B}_0 + \boldsymbol{B}_1$, $\boldsymbol{J} \approx \boldsymbol{J}_0 + \boldsymbol{J}_1$. The three classical circuit elements have been identified as electromagnetic systems whose solutions correspond to certain combinations of the zero-order and first-order solutions of (23)–(26). For example, a *resistor* has been identified to be an electromagnetic system whose first-order fields are negligible compared to its zero-order fields, so that its characterization can be interpreted as an *instantaneous* (memoryless) relationship between the two zero-order fields $\boldsymbol{E}_0$ and $\boldsymbol{H}_0$. In contrast to this, an *inductor* has been identified to be an electromagnetic system where only the first-order magnetic field is negligible. In this case, the electromagnetic system can be interpreted as an inductor in series with a resistor. Similarly, a *capacitor* has been identified to be an electromagnetic system where only the first-order electric field is negligible. In this case, the electromagnetic system can be interpreted as a capacitor in parallel with a resistor. The remaining case where both first-order fields are *not* negligible has been dismissed as having no corresponding situation in circuit theory [12]. We will now offer the suggestion that this missing combination is precisely that which gives rise to the characterization of a memristor.

In order to add more weight to the above interpretation, we will now show that under appropriate conditions the *instantaneous* value of the first-order electric flux density $\boldsymbol{D}_1$ [whose surface integral is proportional to the charge $q(t)$] is related to the *instantaneous* value of the first-order magnetic flux density $\boldsymbol{B}_1$ [whose surface integral is proportional to the flux-linkage $\varphi(t)$]. This would be the case if we postulate the existence of a two-terminal device with the following two properties. 1) Both zero-order fields are negligible compared to the first-order fields; namely, $\boldsymbol{E} \approx \boldsymbol{E}_1$, $\boldsymbol{H} \approx \boldsymbol{H}_1$, $\boldsymbol{D} \approx \boldsymbol{D}_1$, $\boldsymbol{B} \approx \boldsymbol{B}_1$, and $\boldsymbol{J} \approx \boldsymbol{J}_1$. 2) The material from which the device is made is *nonlinear*. To be completely general, we will denote the nonlinear relationships by[10]

$$\boldsymbol{J}_1 = \mathcal{J}(\boldsymbol{E}_1) \tag{27}$$

$$\boldsymbol{B}_1 = \mathcal{B}(\boldsymbol{H}_1) \tag{28}$$

$$\boldsymbol{D}_1 = \mathcal{D}(\boldsymbol{E}_1) \tag{29}$$

where $\mathcal{J}(\cdot)$, $\mathcal{B}(\cdot)$, and $\mathcal{D}(\cdot)$ are one-to-one continuous functions from R^3 *onto* R^3. Under these assumptions, (26) and (27) can be combined to give

$$\text{curl } \boldsymbol{H}_1 = \mathcal{J}(\boldsymbol{E}_1). \tag{30}$$

Observe that (30) does not contain any time derivative. Hence, under any specified boundary condition appropriate for the device, the first-order electric field $\boldsymbol{E}_1$ is related to the first-order magnetic field $\boldsymbol{H}_1$ by a functional relation; namely

$$\boldsymbol{E}_1 = \boldsymbol{f}(\boldsymbol{H}_1). \tag{31}$$

If we substitute (31) for $\boldsymbol{E}_1$ in (29) and then substitute the inverse function of $\mathcal{B}(\cdot)$ from (28) into the resulting expression, we obtain

$$\boldsymbol{D}_1 = \mathcal{D} \circ \boldsymbol{f} \circ [\mathcal{B}^{-1}(\boldsymbol{B}_1)] \equiv \boldsymbol{g}(\boldsymbol{B}_1). \tag{32}$$

Equation (32) specified the instantaneous (memoryless) relationship between $\boldsymbol{D}_1$ and $\boldsymbol{B}_1$; it can be interpreted as the quasi-static representation of the electromagnetic field quantities of the memristor.

To summarize, we offer the interpretation that the physical mechanism characterizing a memristor device must come from the instantaneous (memoryless) interaction between the first-order electric field and the first-order magnetic field of some appropriately fabricated device so that it possesses the two properties prescribed above. This interpretation implies that a physical memristor device is essentially an *ac device*, for otherwise, its associated dc electromagnetic fields will give rise to *nonnegligible* zero-order fields. This requirement is consistent with the circuit-theoretic properties of the memristor, for a dc current source would give rise to an infinite charge [$q(t) \to \infty$ as $t \to \infty$] and a dc voltage source would give rise to an infinite flux-linkage [$\varphi(t) \to \infty$ as $t \to \infty$]. This requirement is, of course, intuitively reasonable. After all, we do not connect a dc voltage source across an inductor. Nor do we connect a dc current source across a capacitor!

V. Some Novel Applications of Memristors

The voltage and current waveforms of the simple memristor circuit shown in Fig. 5 are rather peculiar and are certainly not typical of those normally observed in *RLC* circuits. This observation suggests that memristors might give rise to some novel applications outside those for *RLC* circuits. Our objective in this section is to present a number of interesting examples which might indicate the potential usefulness of memristors.

A. Applications of Memristors to Device Modeling[11]

Although many unconventional devices have been invented in the last few years, the physical operating principles of most of these devices have not yet been fully understood. In order to analyze circuits containing these devices, a

[10] In the case of isotropic material, (27)–(29) reduce to $\boldsymbol{J}_1 = \sigma(\boldsymbol{E}_1)\boldsymbol{E}_1$, $\boldsymbol{B}_1 = \mu(\boldsymbol{H}_1)\boldsymbol{H}_1$, and $\boldsymbol{D}_1 = \epsilon(\boldsymbol{E}_1)\boldsymbol{E}_1$, where the coefficients $\sigma(\cdot)$, $\mu(\cdot)$, and $\epsilon(\cdot)$ are the *nonlinear conductivity*, *nonlinear magnetic permeability*, and *nonlinear dielectric permittivity* of the material.

[11] The author is grateful to one of the reviewers who pointed out that a charge-controlled memristor has been used in the modeling of varactar diodes [13], [14].

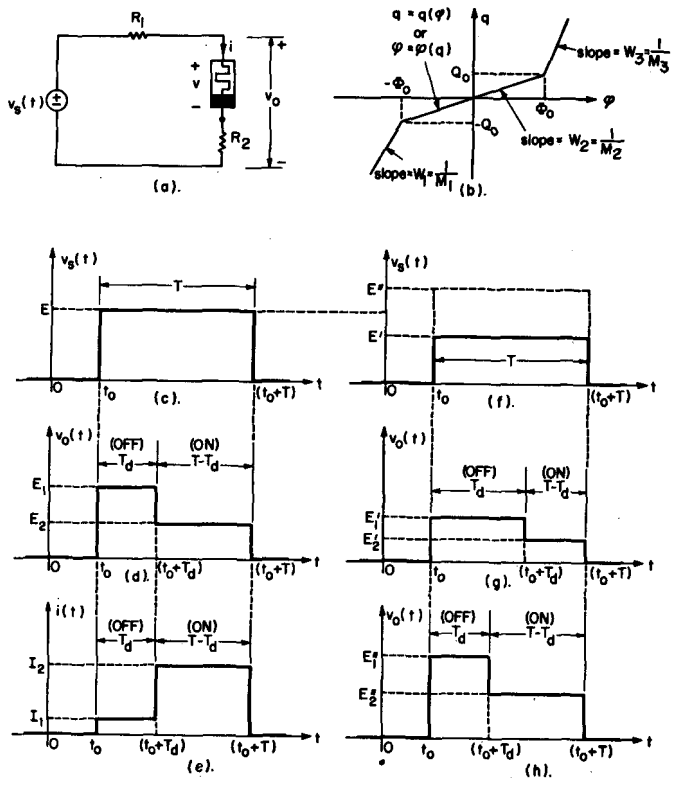

Fig. 6. Output voltage waveform $v_o(t)$ of simple memristor circuit shown in (a) corresponding to a stepwise input voltage $v_s(t)$ of different amplitudes bears a striking resemblance to corresponding waveforms of the same circuit but with the memristor replaced by typical amorphous ovonic threshold switch.

realistic "circuit model" must first be found. We will now show that the *memristor* can be used to model the properties of two recently discovered, but unrelated, devices.

Example 1: Modeling an Amorphous "Ovonic" Threshold Switch

An amorphous "ovonic" threshold switch is a two-terminal device which uses an amorphous glass rather than the more common crystalline semiconductor material used in most solid-state devices [15]–[17]. This device has already attracted much international attention because of its potential usefulness [18], [19]. To show that the memristor provides a reasonable model for at least one type of the amorphous devices, let us consider the memristor circuit shown in Fig. 6(a), where the φ–q curve of the memristor is shown in Fig. 6(b).[12] From Theorem 5 we know the order of complexity of this circuit is equal to one. The state equation is given by

$$dq/dt = v_s(t)/[R_1 + R_2 + M(q)]. \tag{33}$$

Since the variables are separable, the solution is readily found to be

$$\boxed{q(t) = h^{-1} \circ \left(\int_{t_0}^{t} v_s(\tau)\, d\tau + \varphi(q(t_0)) \right)} \tag{34}$$

where

$$\boxed{h(q) \equiv (R_1 + R_2)q + \varphi(q)} \tag{35}$$

and $\varphi = \varphi(q)$ represents the φ–q curve of the memristor shown in Fig. 6(b). Observe that $h(q)$ is a strictly monotonically increasing function of q; hence, its inverse $h^{-1}(\cdot)$ always exists. The output voltage $v_o(t)$ is readily found to be given by

$$v_o(t) = v_s(t) - R_1[dq(t)/dt]. \tag{36}$$

If we let $v_s(t)$ be a square-wave pulse, as shown in Fig. 6(c), and let $q(t_0) = 0$, where t_0 is the initial time, then the output waveforms $v_o(t)$ and $i(t)$, corresponding to the memristor φ–q curve shown in Fig. 6(b), can be derived from (34)–(36); they are shown in Fig. 6(d) and (e). These output waveforms are completely characterized by the following parameters:

$$E_1 = [(M_2 + R_2)/(M_2 + R_1 + R_2)]E \tag{37}$$

$$E_2 = [(M_3 + R_2)/(M_3 + R_1 + R_2)]E \tag{38}$$

$$I_1 = E/(M_2 + R_1 + R_2) \tag{39}$$

$$I_2 = E/(M_3 + R_1 + R_2) \tag{40}$$

$$T_d = [\Phi_0 + (R_1 + R_2)Q_0]/E \tag{41}$$

where M_2 and M_3 represent the memristance corresponding to segments 2 and 3 of the memristor φ–q curve and where (Φ_0, Q_0) is the coordinate of the breakpoint between these two segments. An examination of (41) shows that for a given φ–q curve, the *time delay T_d decreases as the amplitude E of the square-wave pulse in Fig. 6(c) increases.* Hence, corresponding to the three square-wave pulses with amplitude E, E', and E'' ($E' < E < E''$) shown in Fig. 6(c) and (f), we obtain the waveforms for the output voltage $v_o(t)$ as shown in Fig. 6(d), (g), and (h), respectively. A comparison between these waveforms with the corresponding published waveforms for the ovonic threshold switch reveals a striking resemblance [15], [16]. The memristor with the φ–q curve shown in Fig. 6(b) seems to simulate not only the exact shape of the stepwise waveforms, but also the attendant decrease of the time delay with increasing values of E.[13]

[12] This circuit is identical to the switching circuit described in [15], [16], but with an ovonic threshold device connected in place of the memristor. As explained in [15], [16], this circuit operates like a switch in the sense that prior to the application of a square-wave pulse, the ovonic switch behaves like a high resistance and is said to be operating in the OFF state. After the pulse is applied, the ovonic switch remains in its OFF state until after some *time delay T_d*; thereupon it switches to a low resistance state. Since the circuit is essentially a voltage divider, the output voltage $v_o(t)$ will be high when the ovonic switch is operating in its OFF state, and will be low when it is operating in its ON state.

[13] Since the author has been unable to obtain a sample of an ovonic threshold switch, the comparisons were made only with published waveforms. It is not clear how well our present memristor model will simulate the rate of decrease of the time delay with increasing values of E. In any event, the *qualitative agreement* with published waveforms is quite remarkable.

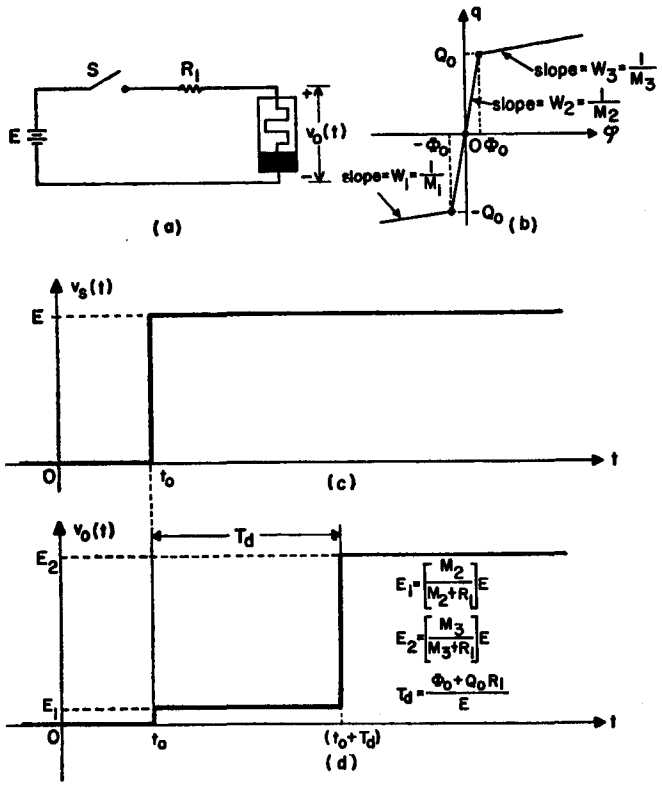

Fig. 7. Output waveform $v_o(t)$ for basic timing circuit in (a) demonstrates that the memristor with φ–q curve shown in (b) provides an excellent circuit model for an E-Cell.

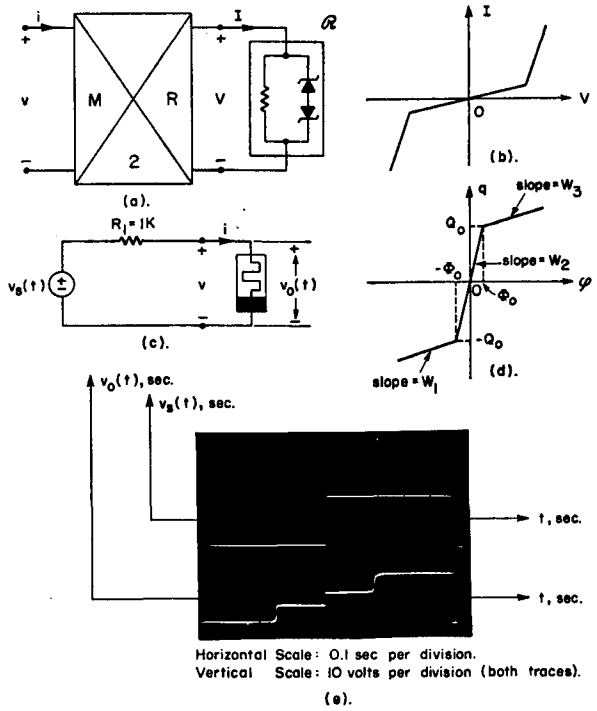

Fig. 8. Practical memristor circuit for generating staircase waveforms.

Example 2: Modeling an Electrolytic E-Cell

An E-Cell (also known as a Coul Cell) is an *electrochemical* two-terminal device [20] capable of producing time delays ranging from seconds to months. An E-Cell can be considered as a subminiature electrolytic plating tank consisting of three basic components, namely, an *anode*, *a cathode*, and an *electrolyte*. The anode, usually made of gold, is immersed in the electrolyte solution which in turn is housed within a silver can that also serves as the cathode. The time delay is controlled by the initial quantity of silver that has been previously plated from the cathode onto the anode and the operating current. During the specified *timing interval* silver ions will be transferred from the anode to the cathode, and the E-Cell behaves like a linear resistor with a *low resistance*. The end of the timing interval corresponds to the time in which all of the silver has been plated off the anode; thereupon the E-Cell behaves like a linear resistor with a *high resistance*. Hence, any reasonable model of an E-Cell must behave like a *time-varying linear* resistor which changes from a low resistance to a high resistance after a dc current is passed through it for a specified period of time equal to the timing interval. We will now show that this behavior can be precisely modeled by a memristor with the φ–q curve shown in Fig. 7(b). To demonstrate the validity of this model, let us analyze the simplest E-Cell timing circuit, shown in Fig. 7(a), but with the E-Cell replaced by a memristor. In practice, the exact amount of silver to be plated is specified by the manufacturer and from this information the circuit is designed so that the correct amount of current will pass through the E-Cell, thereby providing the desired timing interval. The effect of closing the switch S in Fig. 7(a) at $t = t_0$ is equivalent to applying a step input voltage of E volts at t_0, as shown in Fig. 7(c).

Since the circuit in Fig. 7(a) can be obtained from the circuit in Fig. 6(a) upon setting R_2 to zero, we immediately obtain the output voltage $v_o(t)$, as shown in Fig. 7(d). This output voltage waveform is almost identical to the corresponding waveform measured from an E-Cell timing circuit. The timing interval in this model is equal to the time delay T_d. The only discrepancy between this waveform and that actually measured with an E-Cell timing circuit is that, in practice, the rise time is not zero. It always takes a finite but small time interval for an E-Cell to switch completely from a low to a high resistance. The abrupt jump in Fig. 7(d) is, of course, due to the piecewise-linear nature of the assumed φ–q curve. Hence, even the finite switching time can be accurately modeled by replacing the φ–q curve with a curve having a continuous derivative that essentially approximates the piecewise-linear curve.

B. Application of Memristors to Signal Processing

The preceding examples demonstrated that certain types of memristors can be used for switching as well as for delaying signals. Memristors can also be used to process many types of signals and generate various waveforms of practical interest. Due to limitation of space, we will present only one typical application that uses a memristor to generate a *staircase waveform* [21]. This type of waveform has been

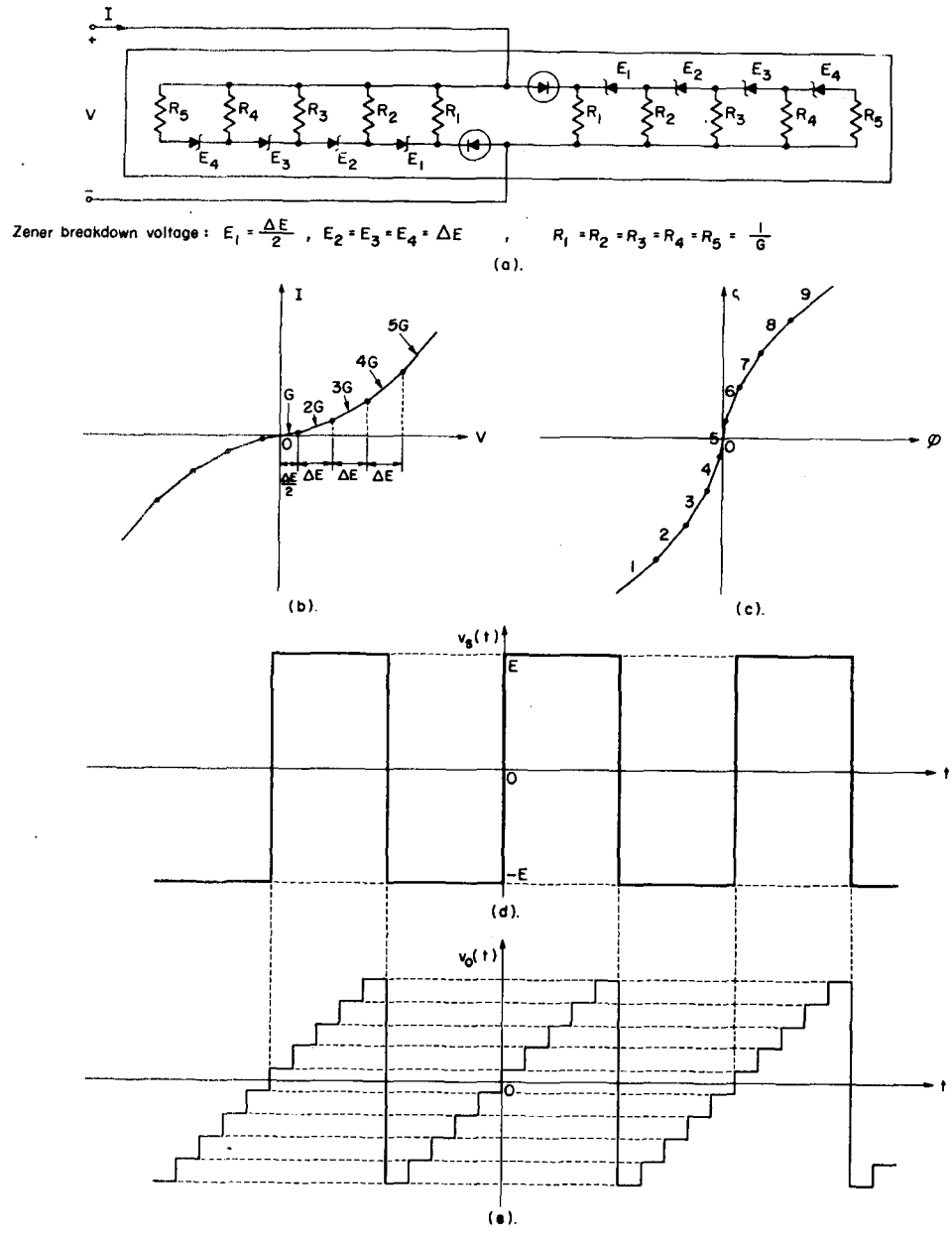

Fig. 9. Nine-segment memristor can be used to generate ten-step staircase periodic waveform.

used in many instruments such as the sampling oscilloscope and the transistor curve tracer.

To simplify discussion, let us consider the design of a four-step staircase waveform generator. The output voltage waveform shown in Fig. 7(d) suggests that a four-step staircase waveform can be generated by driving the circuit in Fig. 7(a) with a symmetrical square wave, provided that a memristor with the φ–q curve shown in Fig. 7(b) is available. This memristor can be synthesized by the methods presented in Section II. In fact, a simple realization is shown in Fig. 8(a) with a nonlinear resistor $\mathfrak{R}$ connected across port 2 of a type-2 M–R mutator. This nonlinear resistor is, in turn, realized by two back-to-back series Zener diodes in parallel with a linear resistor and has a V–I curve as shown in Fig. 8(b). To obtain the desired φ–q curve shown in Fig. 8(d), we connect $\mathfrak{R}$ across port 2 of the type-2 M–R mutator [4]. To verify our design, port 1 of the terminated M–R mutator is connected in series with a square-wave generator $v_s(t)$ and a 1-Ω resistor as shown in Fig. 8(c). The oscilloscope tracings of both the input signal $v_s(t)$ and the output signal $v_o(t)$ are shown in Fig. 8(e). Notice that $v_o(t)$ is indeed a staircase waveform. The finite rise time in going from one step to another is due to the finite resistance of the Zener diode voltage–current characteristic.

It is easy to generalize the above design for generating a staircase waveform with any number of steps. The nonlinear resistor required for generating a ten-step staircase waveform is shown in Fig. 9(a). This circuit consists of two Zener-diode ladder networks connected back to front in parallel [1]. The resulting V–I curve and the corresponding φ–q curve are shown in Fig. 9(b) and (c), respectively. Corresponding to the square-wave input voltage $v_s(t)$ shown in Fig. 9(d), we obtain the ten-step staircase waveform $v_o(t)$ as shown in Fig. 9(e).

VI. Concluding Remarks

The memristor has been introduced as the *fourth* basic circuit element. Three new types of *mutators* have been introduced for realizing memristors in the form of active circuits. An appropriate cascade connection of these mutators and those already introduced in [3] can be used to realize *higher order elements* characterized by a relationship between $v^{(m)}(t)$ and $i^{(n)}(t)$, where $v^{(m)}(t)$ ($i^{(n)}(t)$) denotes the mth (nth) time derivative of $v(t)$ ($i(t)$) if $m>0$ ($n>0$), or the mth iterated time integral of $v(t)$ ($i(t)$) if $m<0$ ($n<0$). Several operational laboratory models of memristors have been built to demonstrate some of the peculiar signal-processing properties of memristors. The application of memristors in modeling unconventional devices shows that memristors are useful even if they are used as a conceptual tool of analysis. While only resistor–memristor circuits have been presented, it is not unreasonable to expect that the most interesting applications will be found in circuits containing resistors, inductors, capacitors, and memristors.

Although no physical memristor has yet been discovered in the form of a physical device without internal power supply, the circuit-theoretic and quasi-static electromagnetic analyses presented in Sections III and IV make plausible the notion that a memristor device with a monotonically increasing φ–q curve could be invented, if not discovered accidentally. It is perhaps not unreasonable to suppose that such a device might already have been fabricated as a laboratory curiosity but was improperly identified! After all, a memristor with a simple φ–q curve will give rise to a rather peculiar—if not complicated hysteretic—v–i curve when erroneously traced in the current-versus-voltage plane.[14] Perhaps, our perennial habit of tracing the v–i curve of any new two-terminal device has already misled some of our device-oriented colleagues and prevented them from discovering the true essence of some new device, which could very well be the missing memristor.

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[14] Moreover, such a curve will change with frequency as well as with the tracing waveform.

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