PERFORMANCE OF A LOW POWER FULLY-DEPLETED DEEP SUBMICRON SOI TECHNOLOGY AND ITS EXTENSION TO 0.15 µm*

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Lincoln Laboratory has developed a fully-depleted silicon-on-insulator (SOI) technology to build integrated circuits designed for very low power operation and fabricated at the limits of optical lithography. A 0.25 µm (drawn gate length) fully-depleted SOI CMOS process technology was established using 248-nm optical lithography for initial process demonstrations, and to identify non-lithographic process integration pinch points and SOI material related issues. Design rules and SPICE parameters have been issued for the 0.25 µm technology and a multi-project chip set assembled with circuits submitted by 15 organizations external to Lincoln Laboratory. The process technology has been adapted to Lincoln's 193-nm step-and-scan tool (1) to fabricate 0.2 µm circuits and provide the first application of 193-nm lithography to a complete CMOS process. This paper describes the performance characteristics of the technology and the enhancements necessary to extend it to 0.15 µm.

The 0.25 µm fully depleted CMOS-SOI technology is designed for 0.9 volt operation and was developed by utilizing process and device design analytical techniques(2) previously developed for a 0.4 µm bulk CMOS technology. The major features of the technology are thinning of the SOI layer by oxidation to 50 nm, island isolation by silicon etching, sidewall implantation to suppress edge leakage, an 8 nm gate oxide, dual-doped polysilicon gates, a 150 nm spacer oxide, a $TiSi_2$ salicide, and a titanium nitride, aluminum-silicon, and titanium nitride stack deposited at 500C to fill 0.4 µm contacts. The multi-level metal process includes planarization of a plasma-deposited oxide by chemical-mechanical polishing and deposition of the second metal at 450C to fill 0.5 µm vias. All layers were defined by plasma etch techniques. The devices reported here were fabricated on SIMOX wafers with buried oxides (BOX) of 200 and 380nm.

Ring oscillators and RF amplifiers were constructed with devices which had absolute thresholds less than 0.4 V, inverse subthreshold slopes less than 70 mV/decade, delta-L of 0.03 and 0.11 µm, and normalized saturated transconductances of 0.5 and 0.2×10^7 cm/s for the n and p-channel devices, respectively. Ring oscillators and rf amplifiers with gate lengths of 0.25 µm were fabricated with 248-nm lithography. The bandwidth of a 0.25 µm amplifier was 1.62 GHz. The stage delays of 0.2 and 0.25 µm ring oscillators are shown as functions of the the power supply voltage in Figure 1; both devices had delays less than 80 ps at Vdd=0.9 V. The 0.2 µm circuit was fabricated using the 193-nm tool exclusively and is composed of the smallest all-optically defined transistors fabricated to date. The power delay product of the 0.25 µm osillator with a fanout of three was 0.1 pJ at 1V as shown in Figure 2.

Extension of the technology to 0.15 µm drawn gate lengths requires optimization of the buried oxide and SOI thickness(3). Simulation techniques were used to determine a set of process parameters to satisfy the n-channel device targets listed in Table 1 and the sensitivity of the device properties to a 10% increase in those parameters. The analysis assumed a 5 nm gate oxide and indicated that a moderately-doped drain and a boron halo implanted adjacent to the gate reduced the dependence of threshold on gate length. The results summarized in the table show that drain-source leakage is the parameter most sensitive to process variations, that it is dominated by the channel implant dose, and that it is equally affected by SOI thickness and gate length variations. The % Sensitivity listed for each device parameter in the table is the root sum of the percent change squared. It is shown in Figure 3 and indicates that a thinner BOX reduces the sensitivity of device parameters to variations in BOX and SOI thickness, channel length, and channel implant dose. Cobalt disilicide or raised source-drain structures will be required to reduce the transistor extrinsic series resistance and thereby realize the performance advantages of a 0.15 µm design.

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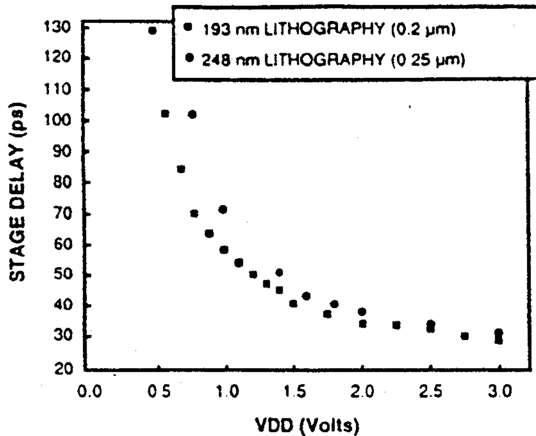

FIGURE 1. STAGE DELAY OF FULLY DEPLETED RING OSCILLATORS

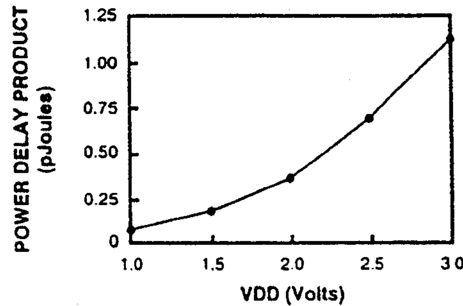

FIGURE 2. POWER DELAY PRODUCT OF A 0.25 µm RING OSCILLATOR

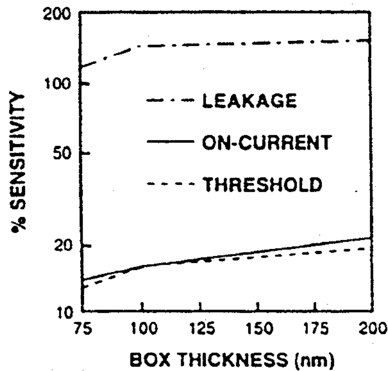

FIGURE 3. SIMULATED DEVICE SENSITIVITY TO BURIED OXIDE THICKNESS; L = 0.15 µm, W = 1 µm

TABLE 1: SIMULATION OF A FULLY DEPLETED 0.15 µm SOI PROCESS

PROCESS FACTOR	NOMINAL VALUE
BOX THICKNESS (nm)	75
SOI THICKNESS (nm)	40
BF2 CHANNEL DOSE (# / cm3)	6.4 e12

SIMULATED DEVICE PARAMETERS:	L = 0.15 µm; W = 1 µm	PARAMETER TARGETS
LEAKAGE (Vd = 1V; Vg = 0V)	100 pa	<100 pa
ON CURRENT (Vd = Vg = 1V)	0.18 ma	>0.2 ma
S (Vd = 0.05V)	73	<70
Vt (Vd = 0.05V)	0.39	<0.4

SENSITIVITY ANALYSIS	% CHANGE DUE TO A 10% PROCESS PARAMETER INCREASE			
PROCESS PARAMETER	LEAKAGE	ON CURRENT	S	Vt
BOX THICKNESS	14%	1%	<1%	−1.3%
SOI THICKNESS	−35%	−3.5%	<1%	5%
BF2 CHANNEL DOSE	−100%	−12%	<1%	10%
GATE LENGTH	−40%	−10%	−2%	3%
% SENSITIVITY	119%	16%	2%	13%

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